

# Mixed Signal Testing Challenges in FPGA- based Radar Systems

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May 17, 2012

# Agenda

## **Introduction: Why Use a Logic Analyzer and Oscilloscope?**

Case Study 1: Linear FM “Chirp” Radar Example

Insertion of Baseband Test Points in the FPGA

FPGA Digital Capture with Logic Analyzer / VSA

Analog IF Capture with Oscilloscope / VSA

Case Study 2: Same Hardware Reconfigured as OFDMA  
Comms System

# Introduction: Why use a logic analyzer and oscilloscope?

With reconfigurable radar designs, whole section is digital and must probe internal to an FPGA

Logic analyzer has capability to automate digital signal capture

Logic analyzer also has ability to export captured data into VSA for analysis

Scope can capture analog IF for export to VSA as well

Allows baseband and RF teams to have common measurement framework

# Agenda

**Introduction: Why Use a Logic Analyzer and Oscilloscope?**

**Case Study 1: Linear FM “Chirp” Radar Example**

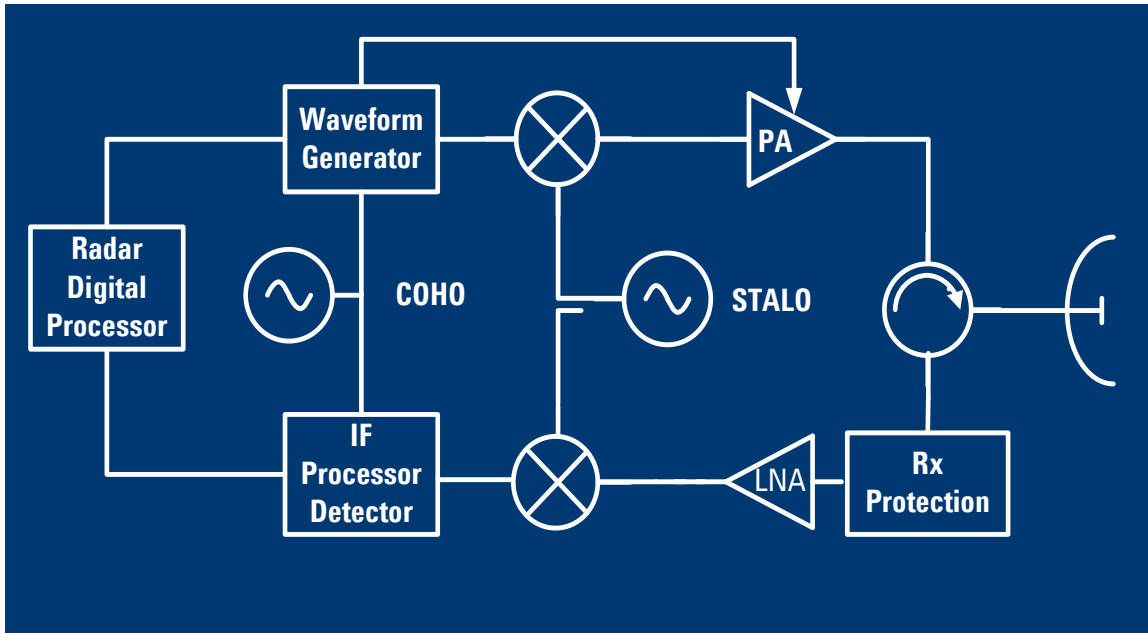
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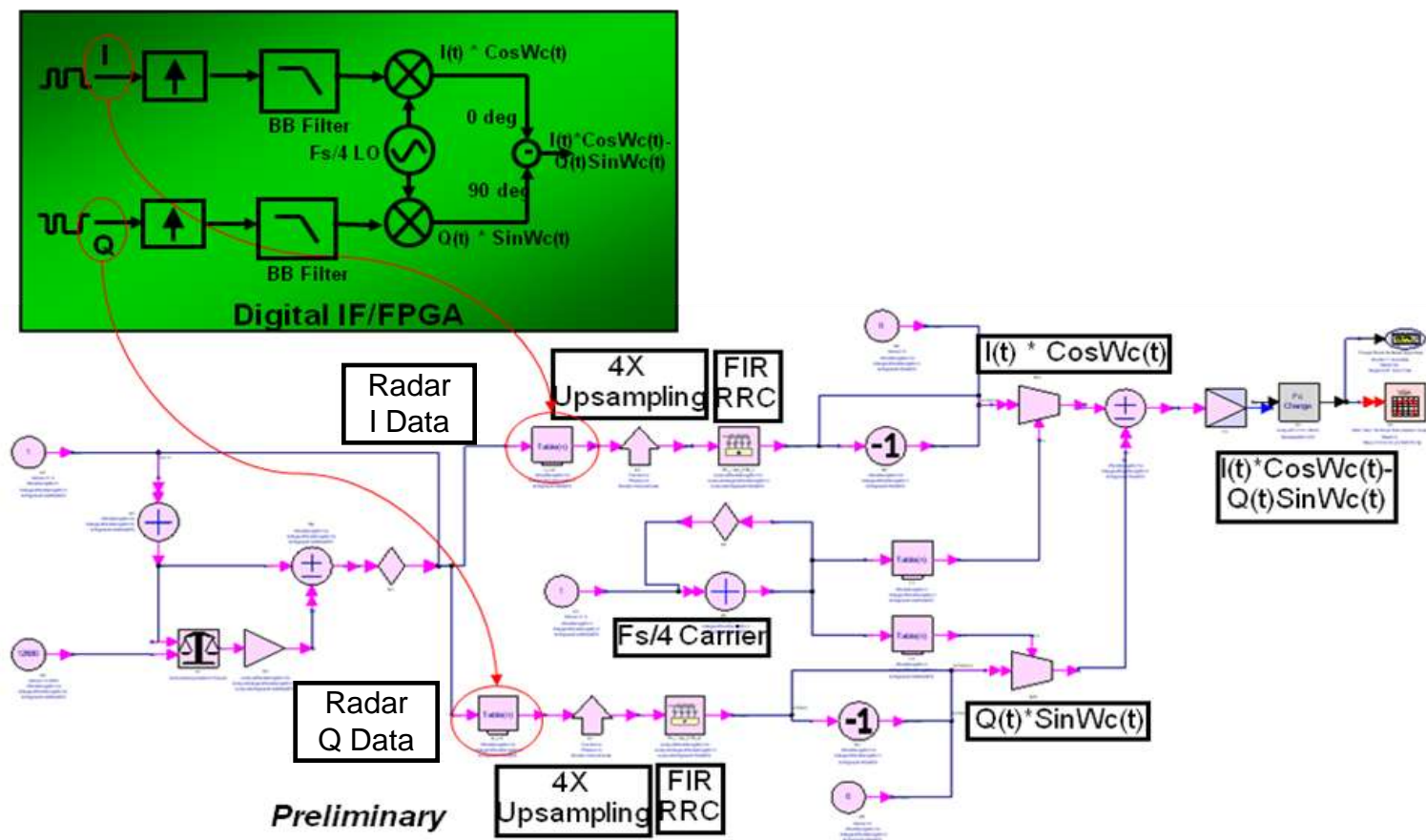
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# Conceptual Block Diagram Re-Configurable Radar Subsystem

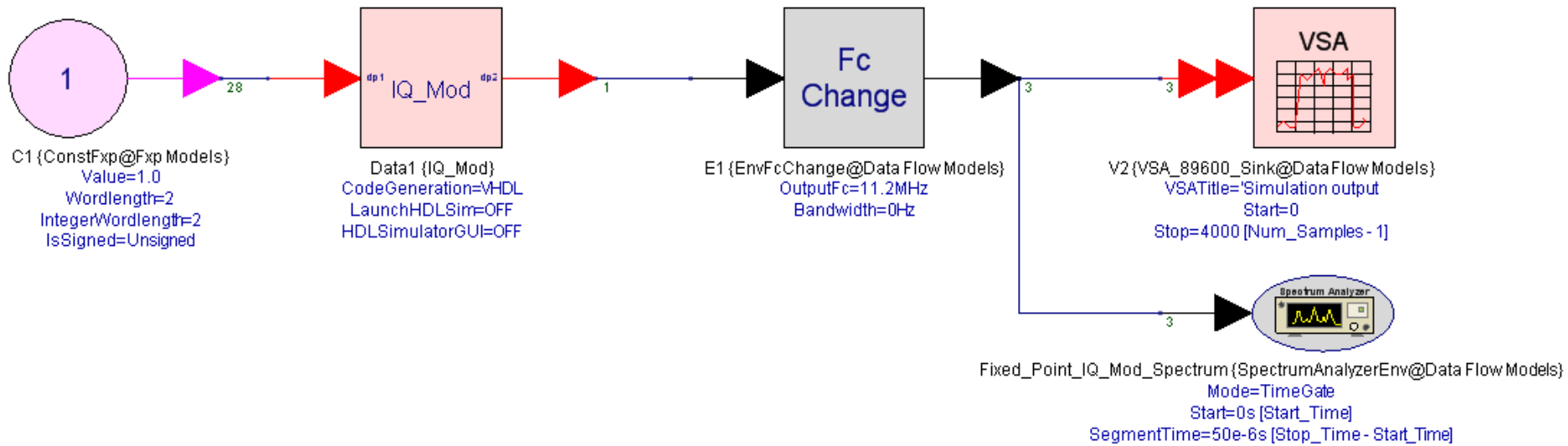


- Radar Digital Processor comprised of FPGAs and DSPs
- May be configurable for different functions
- Consider a case where it is configured as a linear FM (LFM) chirped radar
- Will show common test methodology for FPGA testing | and RF testing

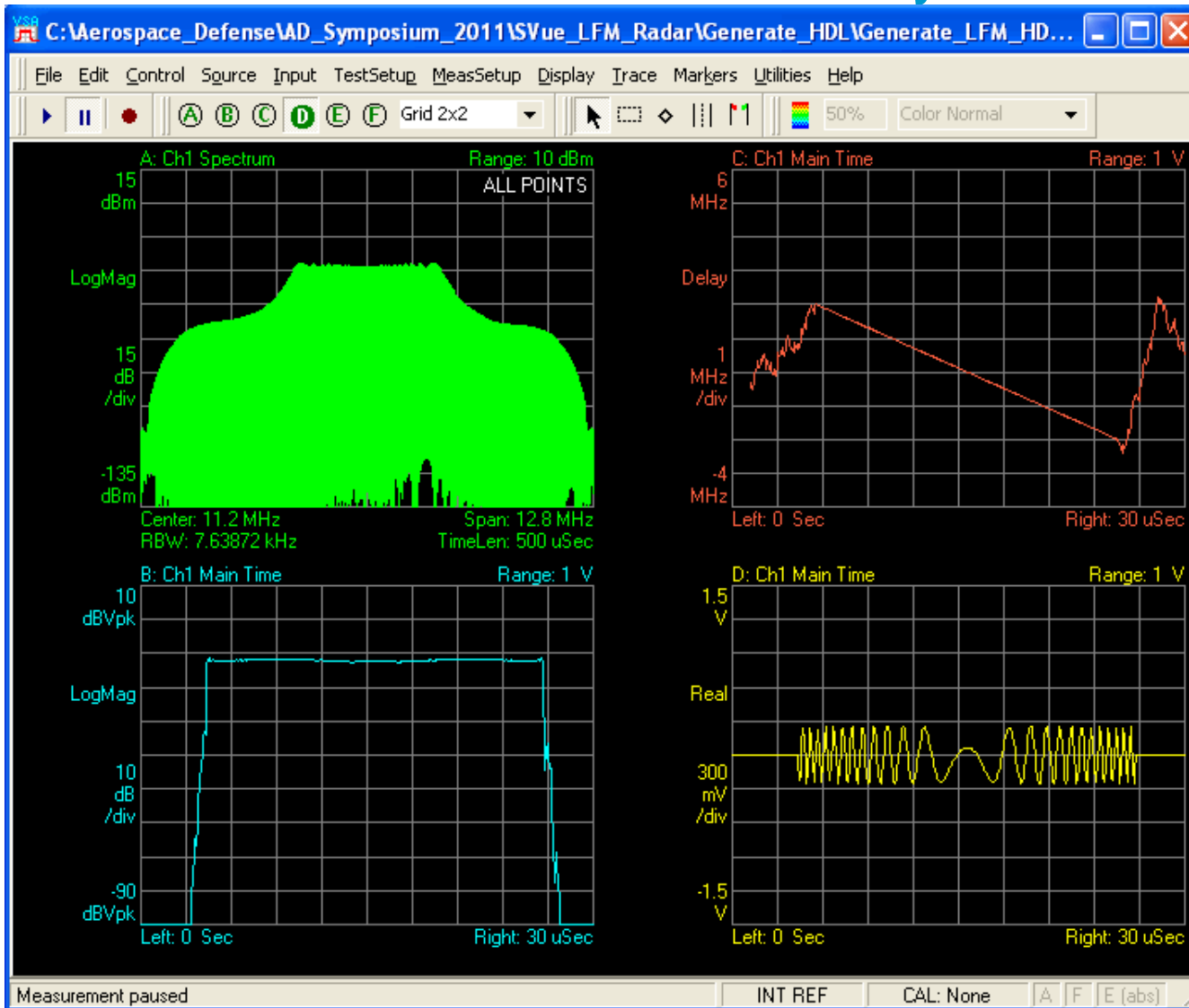
# First Case Study: FPGA LFM Chirp Radar Waveform Design



# Simulation in System Vue



# Simulation Results in System Vue



Expected spectral content

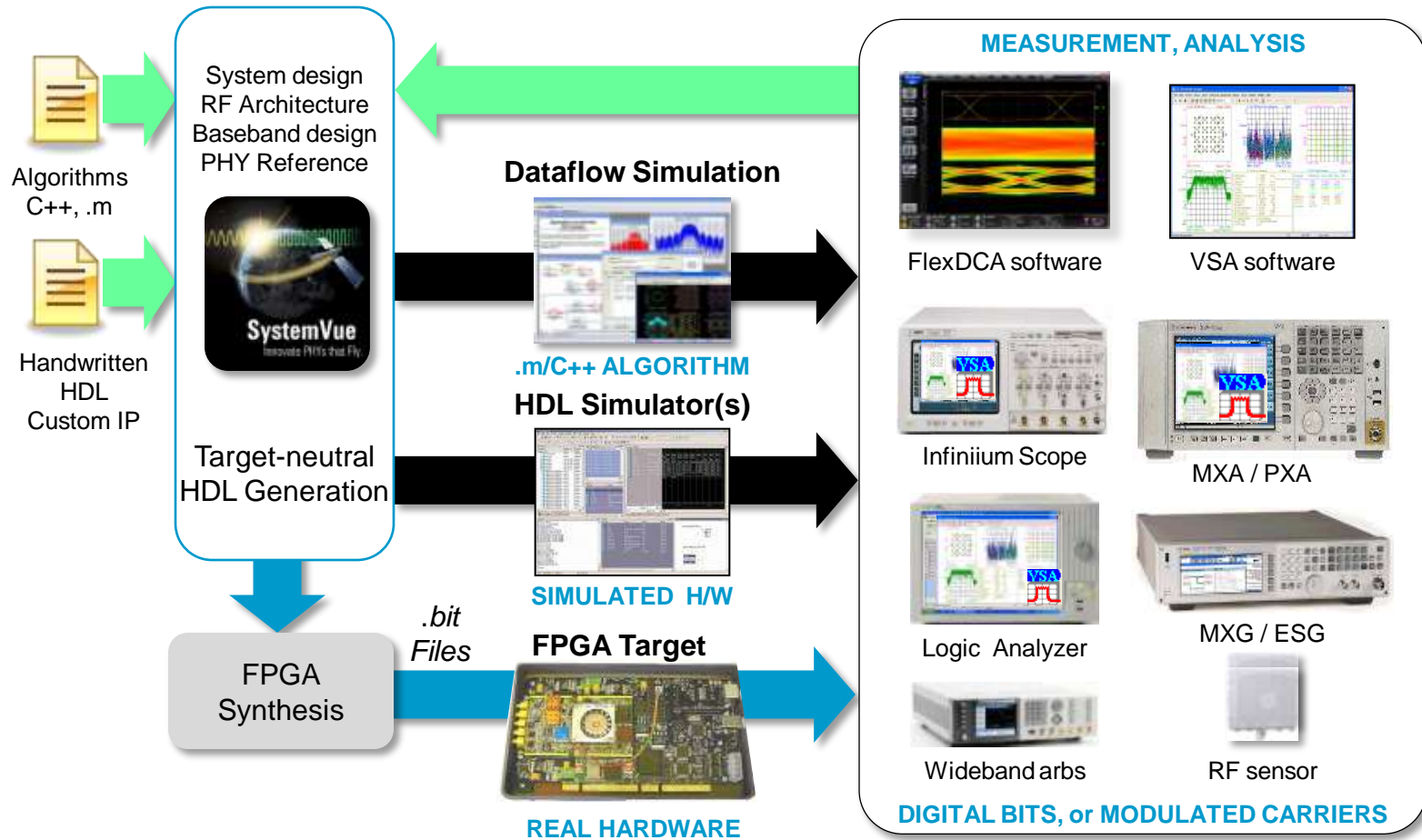
Linear frequency modulation across the pulse profile

Pulse width definition



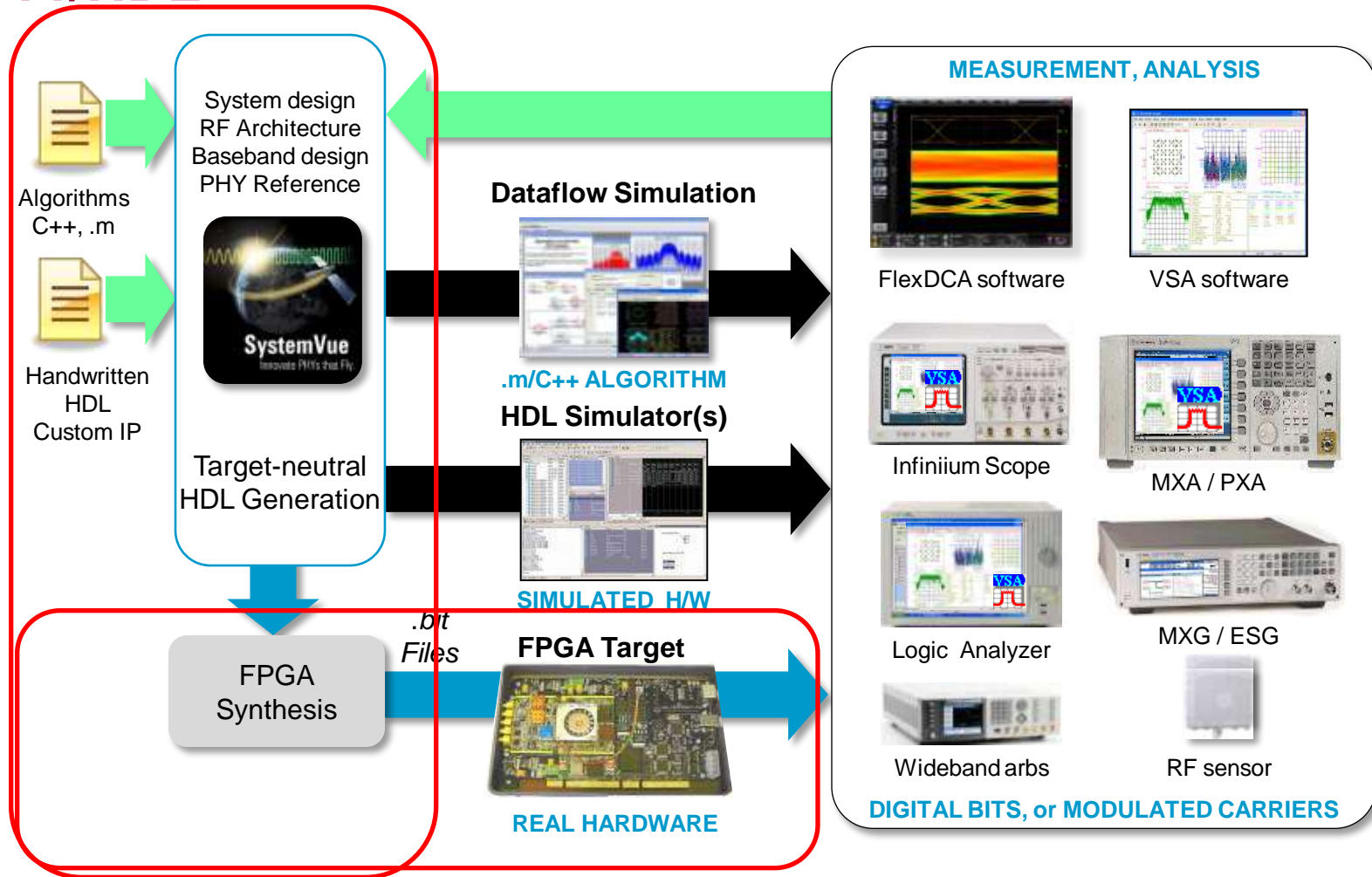
# Integrated, Tops-Down Comms ESL Flow

## Cross-domain model-based design: RF, Comms, and C++/HDL



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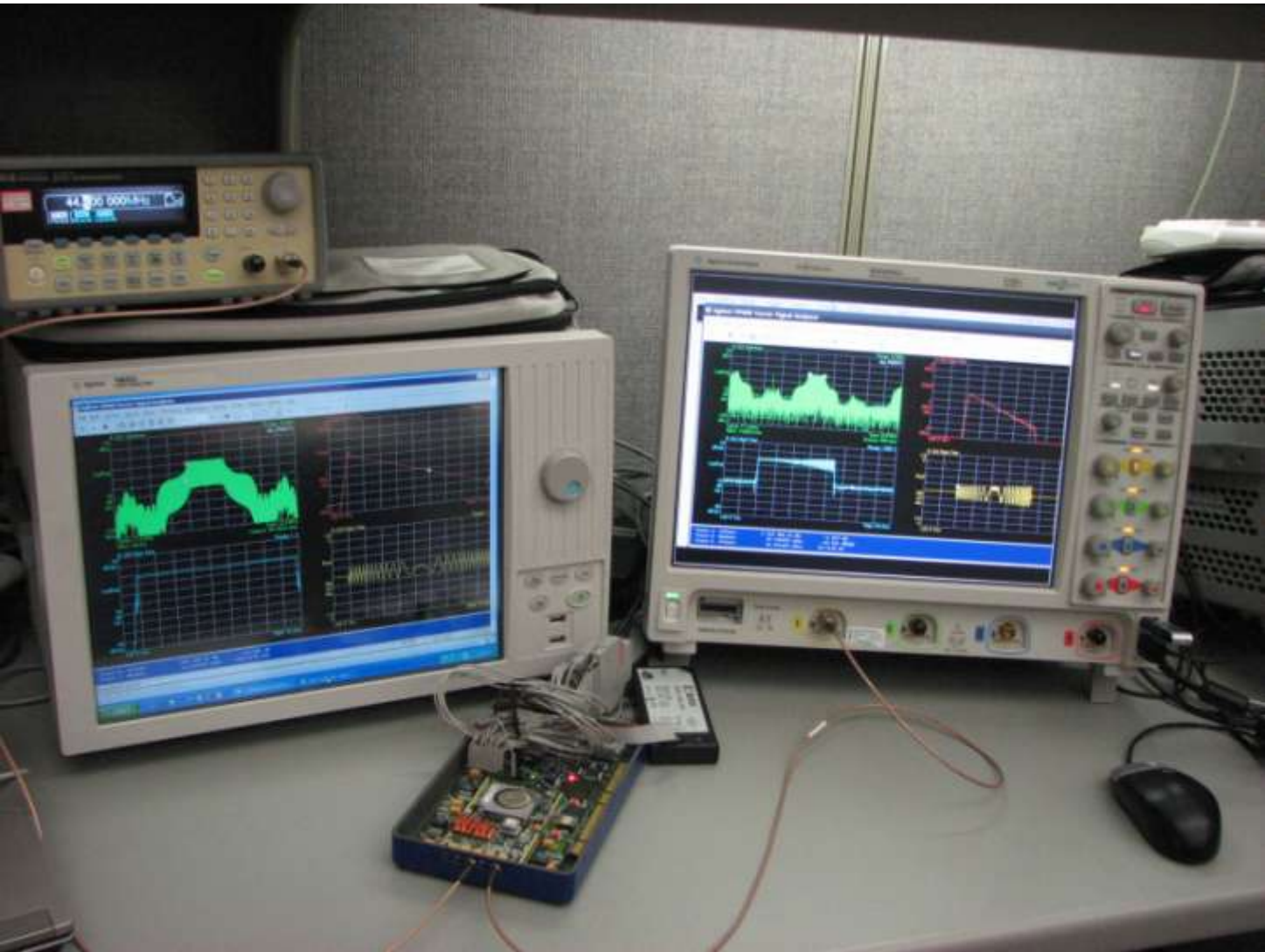
**Insertion of Baseband Test Points in the FPGA**

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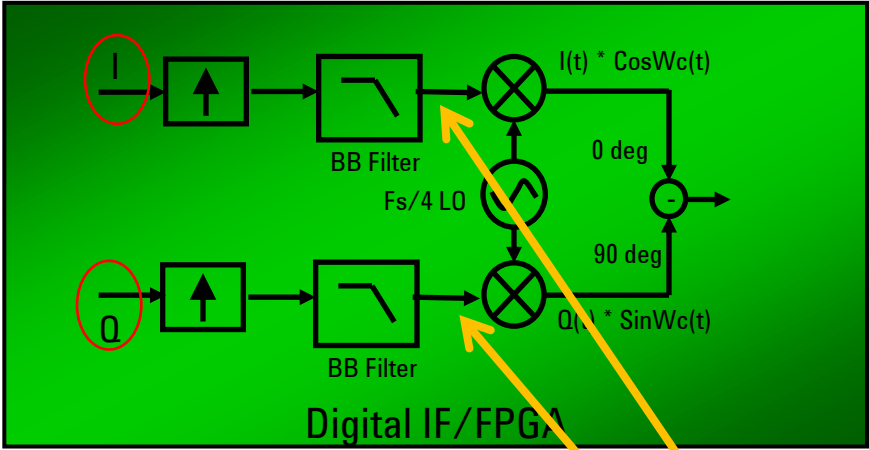
# FPGA LFM Radar Test Setup



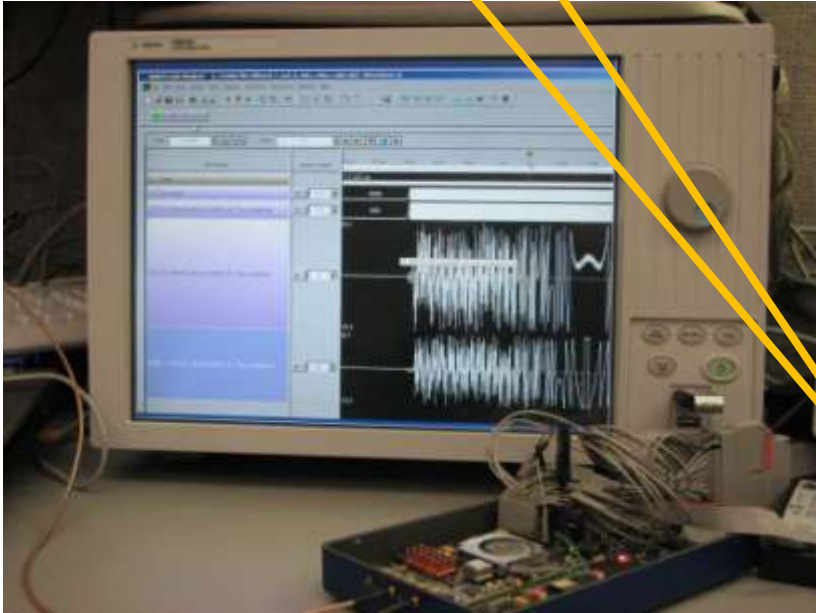
16822A logic analyzer with VSA (L)

MSO9404A oscilloscope with VSA (R)

# Probe Filtered I/Q in FPGA with Dynamic Probe



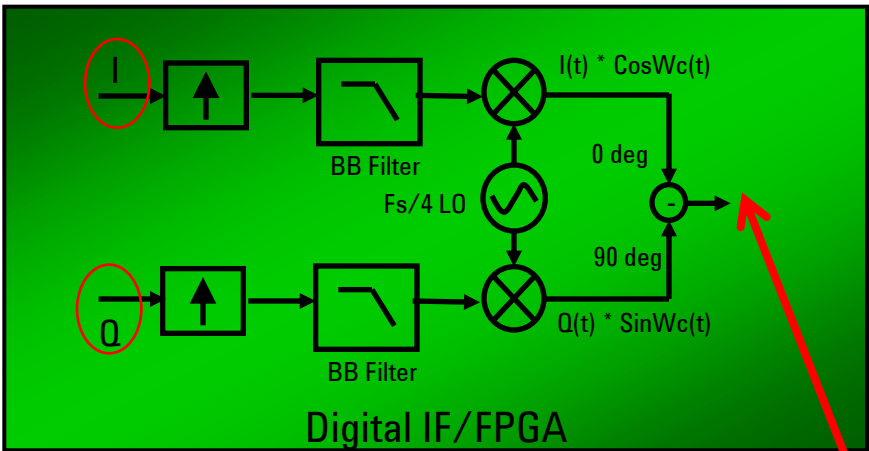
Use Dynamic Probe to Probe FPGA Waveform at Various Stages of the FPGA Implementation



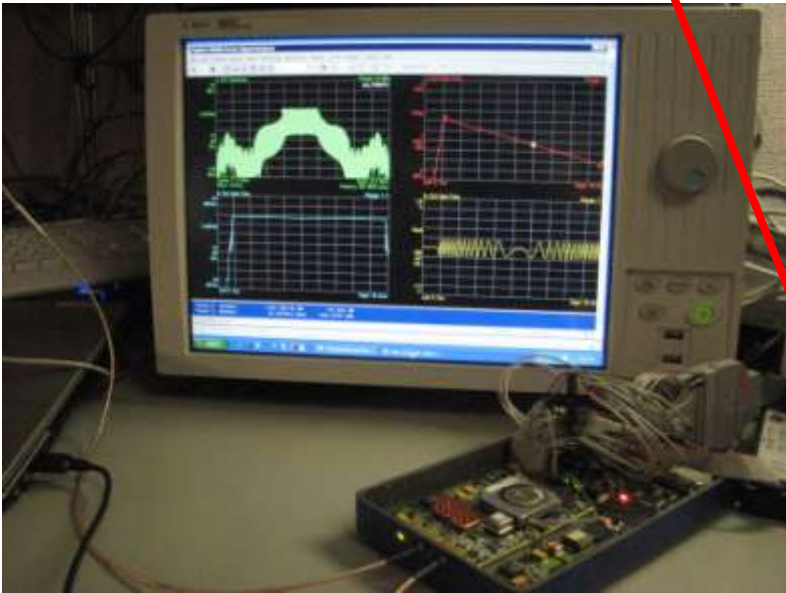
Probes	Modules
Xilinx FPGA Dynamic Probe-1	Slot A My Logic Analyzer-1
FPGA Dynamic Probe Bank Selection	
Core 0	
<ul style="list-style-type: none"> <li>Core 0                     <ul style="list-style-type: none"> <li>IQ_LUT_Outputs_1X</li> <li>FIR_Inputs_1X</li> <li>FIR_Outputs_4X</li> <li><b>DAC_Inputs_4X</b></li> <li>Test Bank</li> </ul> </li> </ul>	



# Probe Digital IF in FPGA with Dynamic Probe



Use Dynamic Probe to Probe FPGA Waveform at Various Stages of the FPGA Implementation



Probes	Modules
Xilinx FPGA Dynamic Probe-1 Properties	Slot A My Logic Analyzer-1
FPGA Dynamic Probe Bank Selection	
Core 0	
Core 0 <ul style="list-style-type: none"><li>IQ_LUT_Outputs_1X</li><li>FIR_Inputs_1X</li><li>FIR_Outputs_4X</li><li>DAC_Inputs_4X</li><li>Test Bank</li></ul>	

# FPGA Measurement Core Configuration

ChipScope Pro Core Inserter [simple\_timing\_core.cdc]

File Edit Help

DEVICE: U0: ATC2

ATC2 Select ATC2 Options

Pin Selection Parameters Net Connections

Global Parameters

Capture Mode: STATE  
Pin Edit Mode: Same as ATCK  
Endpoint Type: SINGLE-ENDED  
TDM Rate: 1X  
Max Frequency Range: 101-200MHz  
ATD Pin Count: 20  
Signal Bank Count: 2  
Data Width: 20

Enable Auto Setup

Defaults

Core Utilization

LUT Count: 264  
FF Count: 373  
BRAM Count: 0

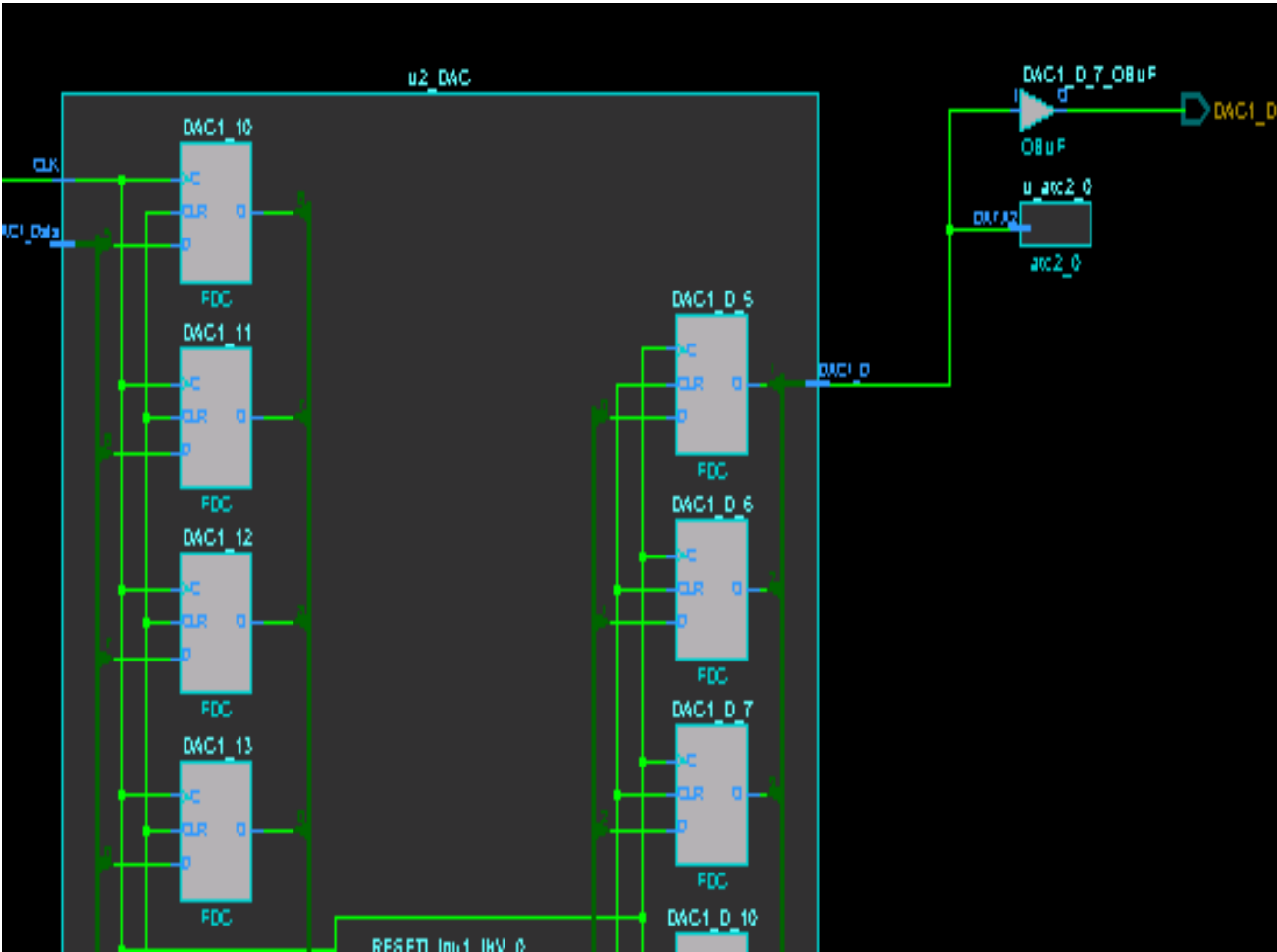
Individual Pin Settings

Pin Name	Pin Loc	IO Standard	vCCO	Drive	Slew Rate
ATCK	J23	LVDCI_25	2.5	N/A	N/A
ATD[0]	L26	LVDCI_25	2.5	N/A	N/A
ATD[1]	M26	LVDCI_25	2.5	N/A	N/A
ATD[2]	M25	LVDCI_25	2.5	N/A	N/A
ATD[3]	M24	LVDCI_25	2.5	N/A	N/A
ATD[4]	M23	LVDCI_25	2.5	N/A	N/A
ATD[5]	M22	LVDCI_25	2.5	N/A	N/A
ATD[6]	M21	LVDCI_25	2.5	N/A	N/A
ATD[7]	M20	LVDCI_25	2.5	N/A	N/A
ATD[8]	N25	LVDCI_25	2.5	N/A	N/A
ATD[9]	N24	LVDCI_25	2.5	N/A	N/A
ATD[10]	M19	LVDCI_25	2.5	N/A	N/A
ATD[11]	N19	LVDCI_25	2.5	N/A	N/A
ATD[12]	K26	LVDCI_25	2.5	N/A	N/A
ATD[13]	K25	LVDCI_25	2.5	N/A	N/A
ATD[14]	L19	LVDCI_25	2.5	N/A	N/A

< Previous Next > Remove Unit

- State or timing core
- Core width
- Assign FPGA physical pins to bring out signals
- Option for time division multiplexing (2x)
- Single ended or differential output

# Xilinx Plan Ahead to Assist in Net Search



- Get graphical view of FPGA implementation
- Helpful to trace signals for probing
- Here can see the bus with the digital IF signal



# Assign FPGA Nets to Each Signal Bank

**Structure / Nets**

- [Toplevel]
- U3\_DCM [dcm\_module]
- U2\_DAC [dac\_module]
- U1\_HDK [IQ\_Mod\_CoSimWrapper]

**Net Name**    **Pattern:**    **Filter**

Net Name	Source Instance	Source Component	Base Type
CLK_FB	Toplevel	Toplevel	PORT
CLK_USER	U3_DCM	dcm_module	BUFG
CONFIG_DONE_OBUF	XST_GND	GND	GND
DAC1_D_0	U2_DAC	dac_module	FDC
DAC1_D_1	U2_DAC	dac_module	FDC
DAC1_D_10	U2_DAC	dac_module	FDC
DAC1_D_11	U2_DAC	dac_module	FDC
DAC1_D_12	U2_DAC	dac_module	FDC
DAC1_D_13	U2_DAC	dac_module	FDC
DAC1_D_2	U2_DAC	dac_module	FDC
DAC1_D_3	U2_DAC	dac_module	FDC
DAC1_D_4	U2_DAC	dac_module	FDC
DAC1_D_5	U2_DAC	dac_module	FDC
DAC1_D_6	U2_DAC	dac_module	FDC
DAC1_D_7	U2_DAC	dac_module	FDC
DAC1_D_8	U2_DAC	dac_module	FDC
DAC1_D_9	U2_DAC	dac_module	FDC

**Net Selections**

**Clock Signals**    **Data Signals**

Channel	Net
CH:0	/U2_DAC/DAC1_D<0>
CH:1	/U2_DAC/DAC1_D<1>
CH:2	/U2_DAC/DAC1_D<2>
CH:3	/U2_DAC/DAC1_D<3>
CH:4	/U2_DAC/DAC1_D<4>
CH:5	/U2_DAC/DAC1_D<5>
CH:6	/U2_DAC/DAC1_D<6>
CH:7	/U2_DAC/DAC1_D<7>
CH:8	/U2_DAC/DAC1_D<8>
CH:9	/U2_DAC/DAC1_D<9>
CH:10	/U2_DAC/DAC1_D<10>
CH:11	/U2_DAC/DAC1_D<11>
CH:12	/U2_DAC/DAC1_D<12>
CH:13	/U2_DAC/DAC1_D<13>
CH:14	/CONFIG_DONE_OBUF
CH:15	/CONFIG_DONE_OBUF
CH:16	/CONFIG_DONE_OBUF
CH:17	/CONFIG_DONE_OBUF
CH:18	/CONFIG_DONE_OBUF
CH:19	/CONFIG_DONE_OBUF

SB0    SB1

Make Connections    Move Nets Up

Remove Connections    Move Nets Down

OK    Cancel

- Go into design hierarchy
- Select nets of interest
- “Make Connections” assigns nets to signal banks
- Also select clock signal

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Insertion of Baseband Test Points in the FPGA

**FPGA Digital Capture with Logic Analyzer / VSA**

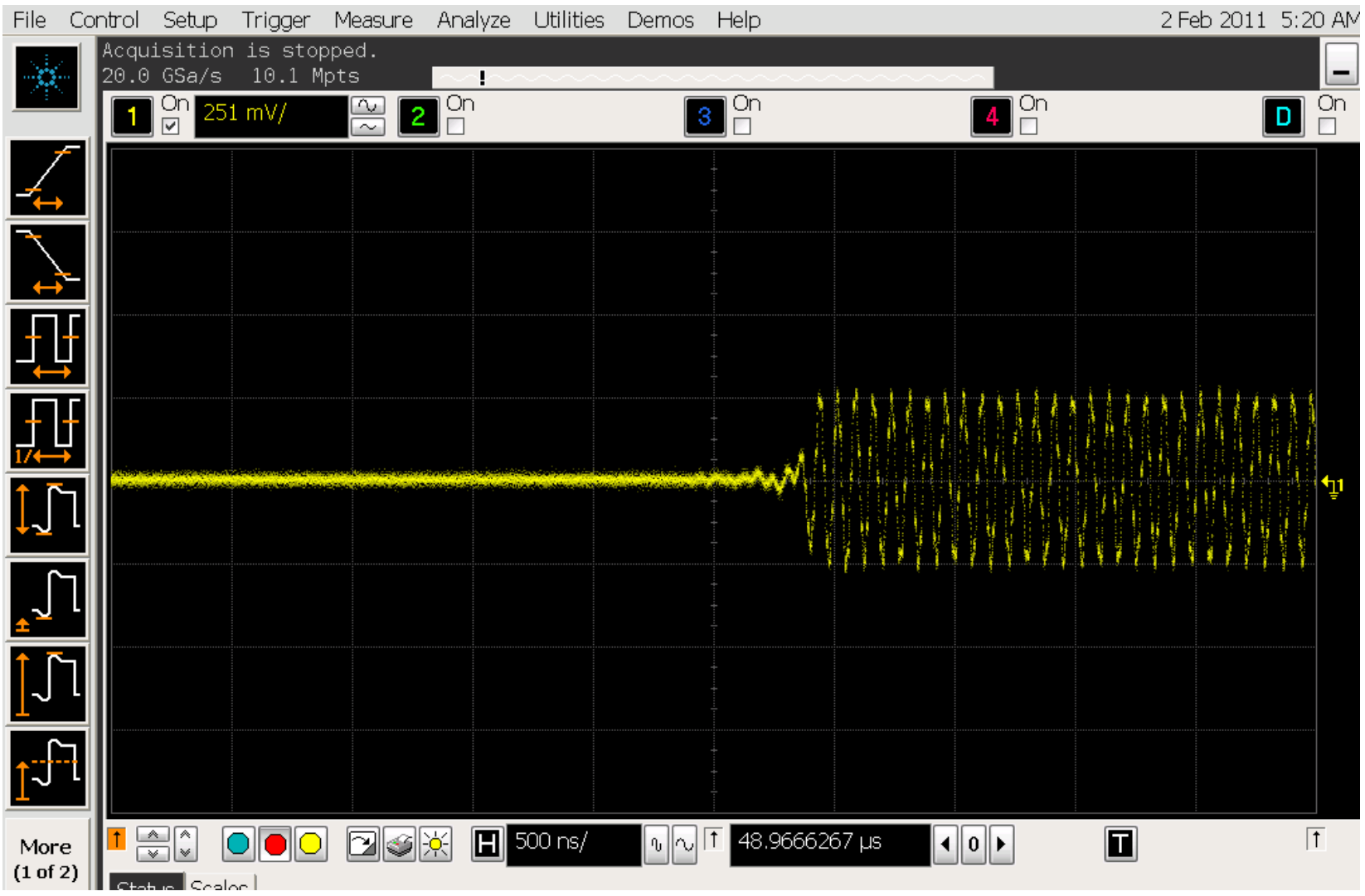
Analog IF Capture with Oscilloscope / VSA

Case Study 2: Same Hardware Reconfigured as OFDMA  
Comms System

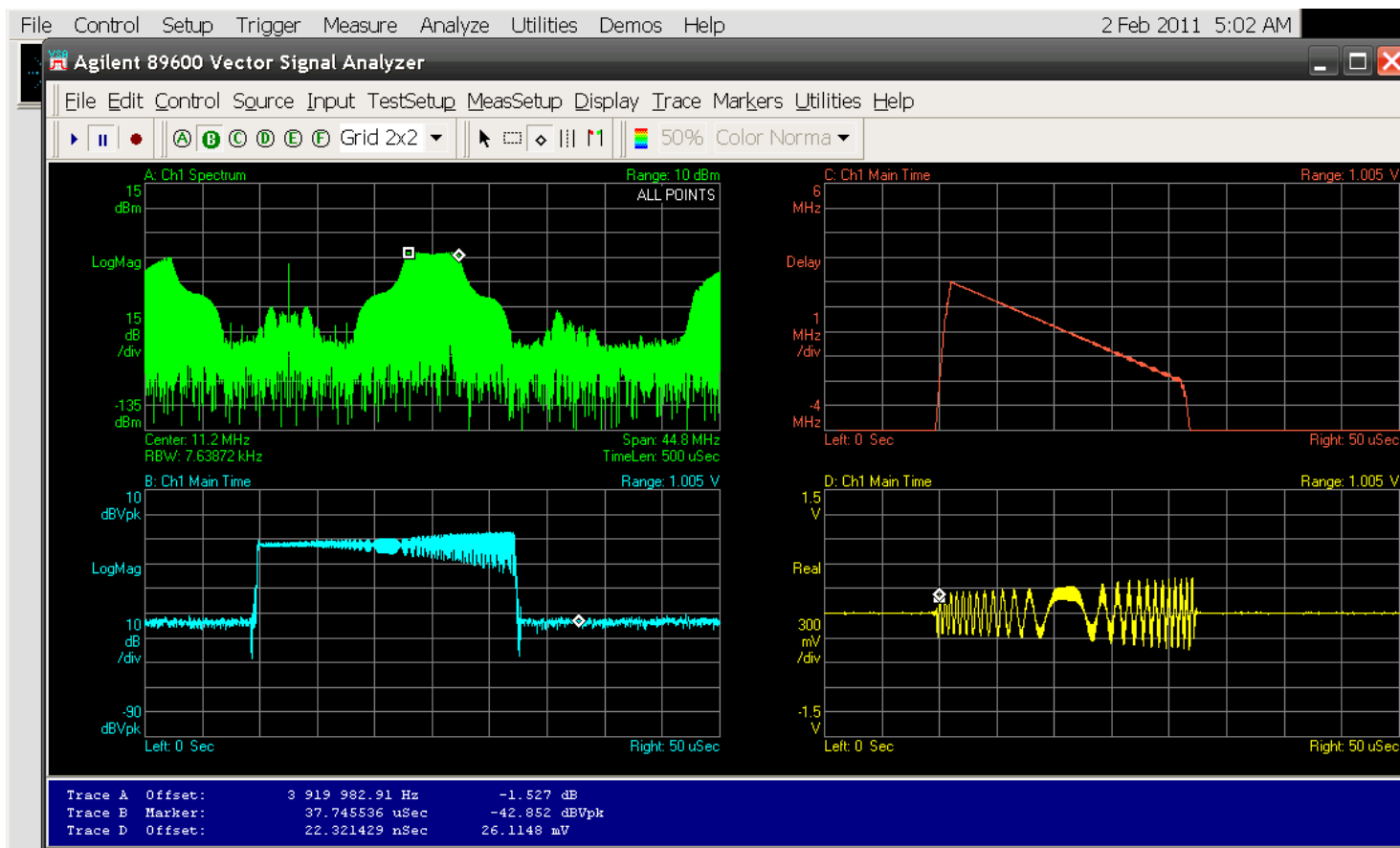
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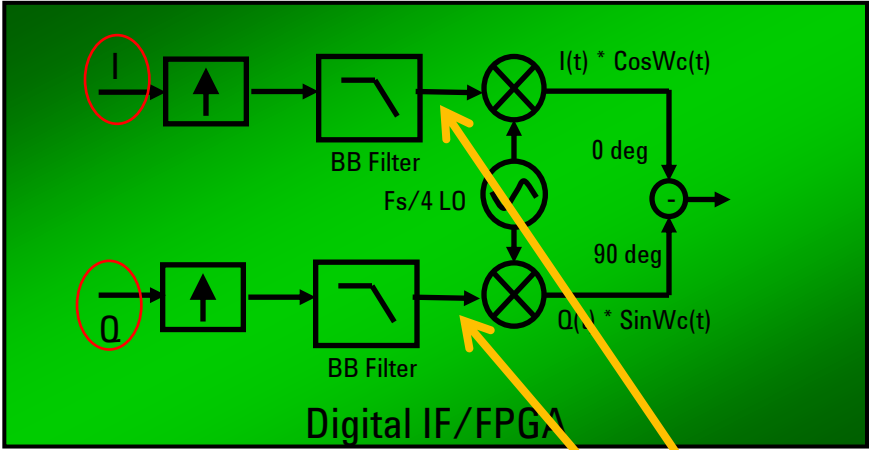
# Capture FPGA LFM Radar Analog IF with Oscilloscope



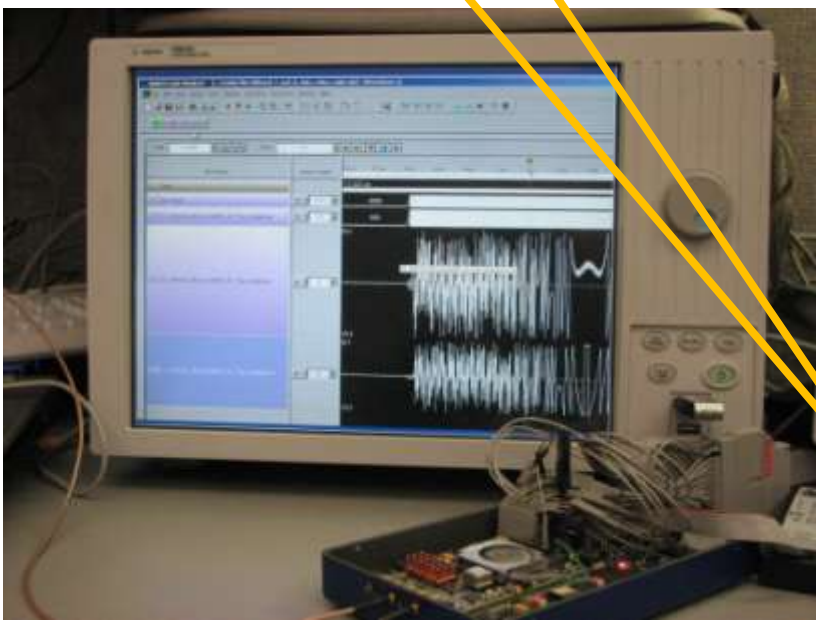
# Analyze LFM Radar Analog IF with VSA Software on Oscilloscope



# Switch to Signal Bank 1 for Filtered Digital I/Q



The Logic Analyzer interface allows the user to switch the FPGA MUX to move the probe points.



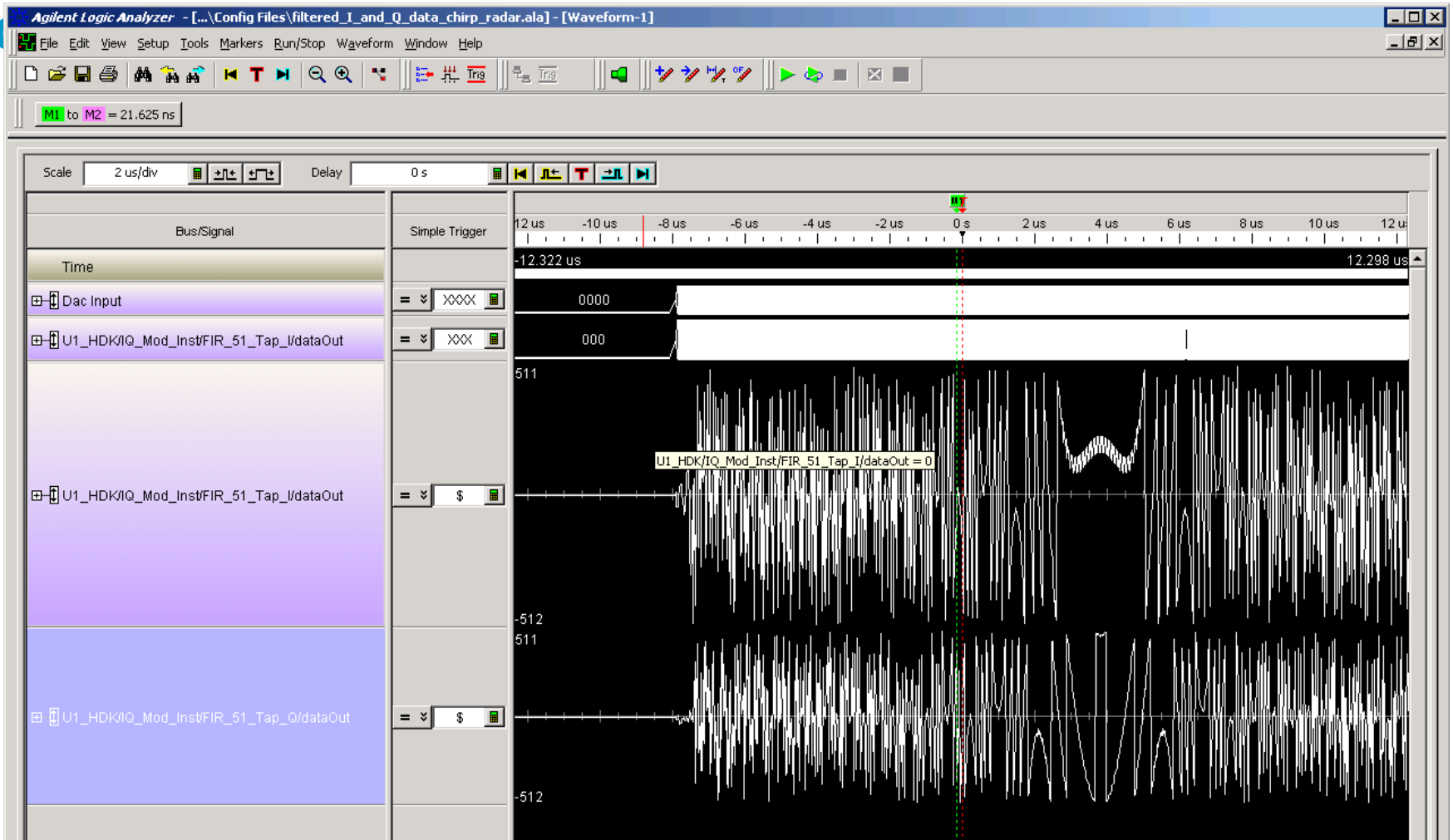
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FPGA Dynamic Probe Bank Selection

Core 0

- Core 0
  - IQ\_LUT\_Outputs\_1X
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  - FIR\_Outputs\_4X
  - DAC\_Inputs\_4X**
  - Test Bank

# Capture FPGA LFM Radar Digital I/Q Waveform with

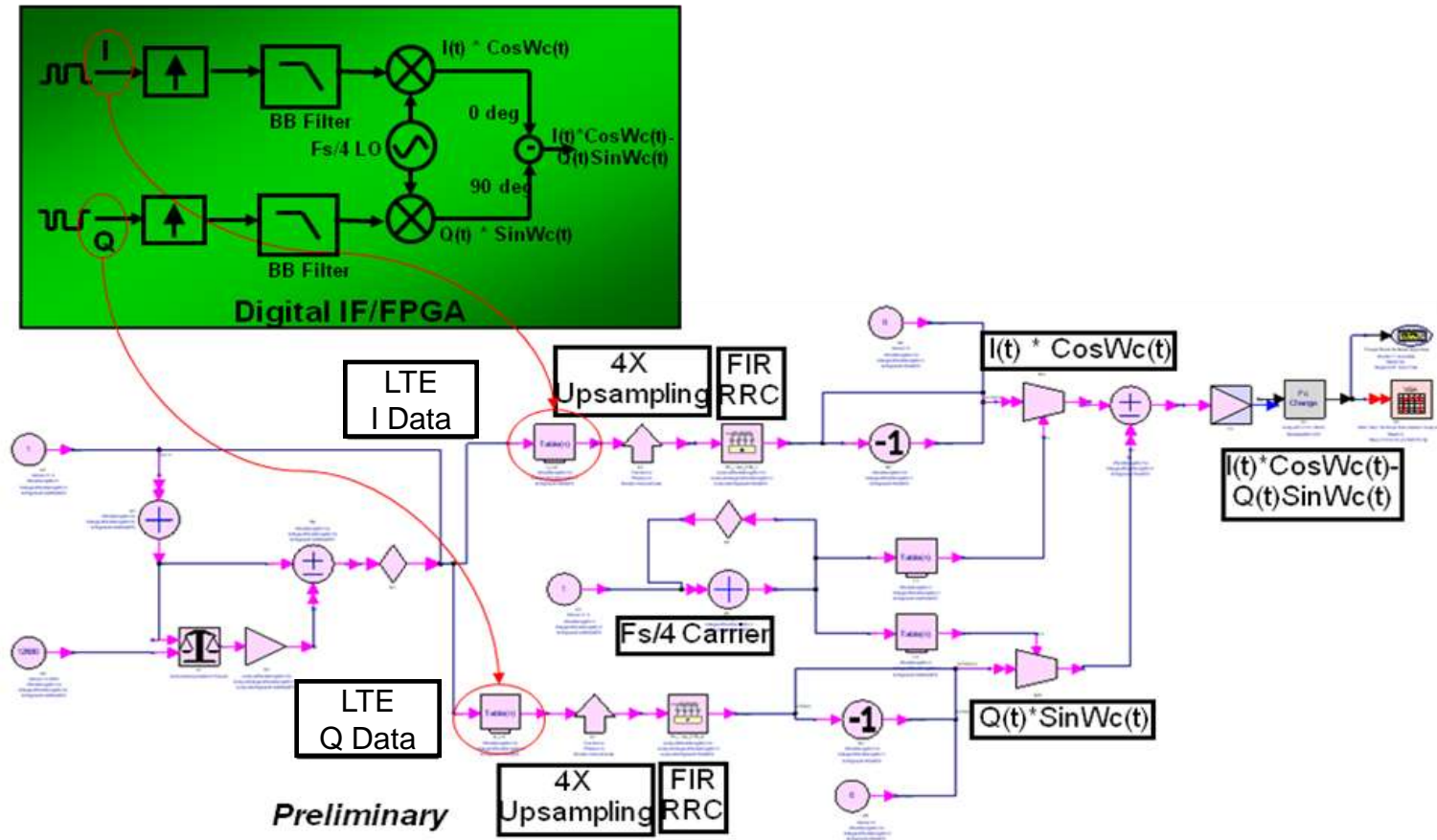


# Agenda

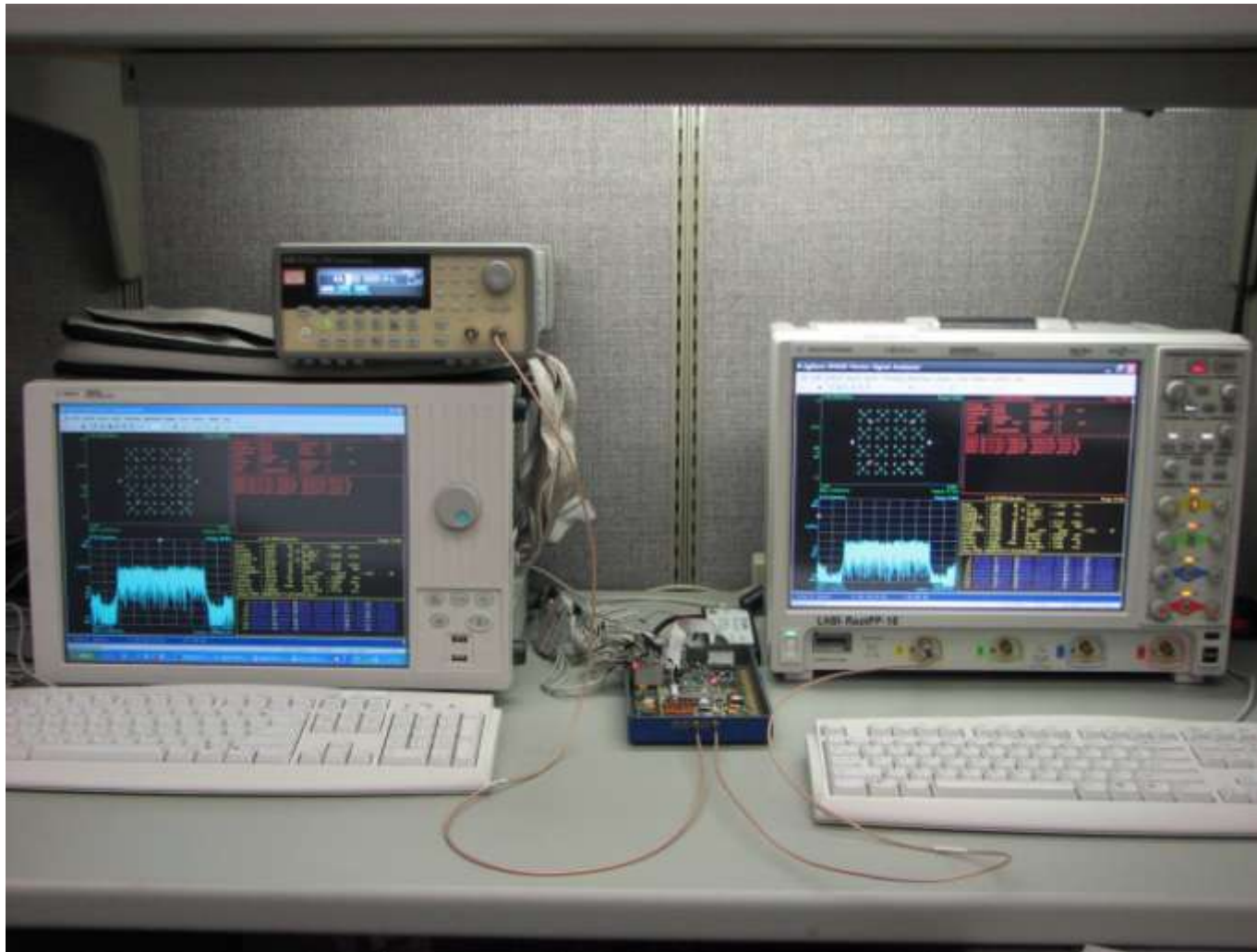
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# Second Case Study: FPGA Comms OFDMA Design



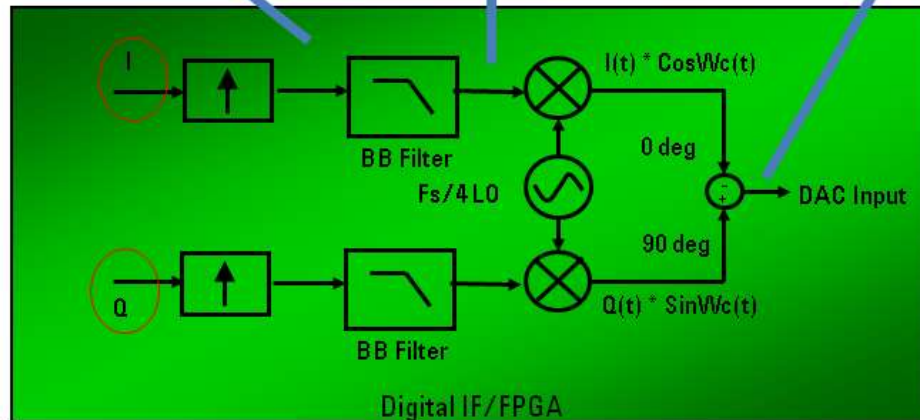
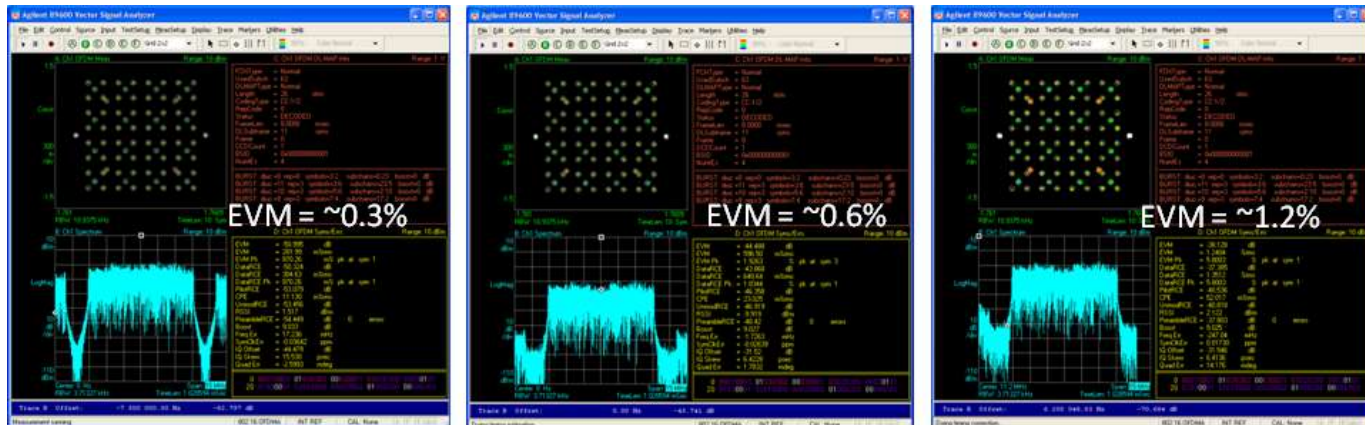
# Second Case Study: FPGA OFDMA Comms Test Setup



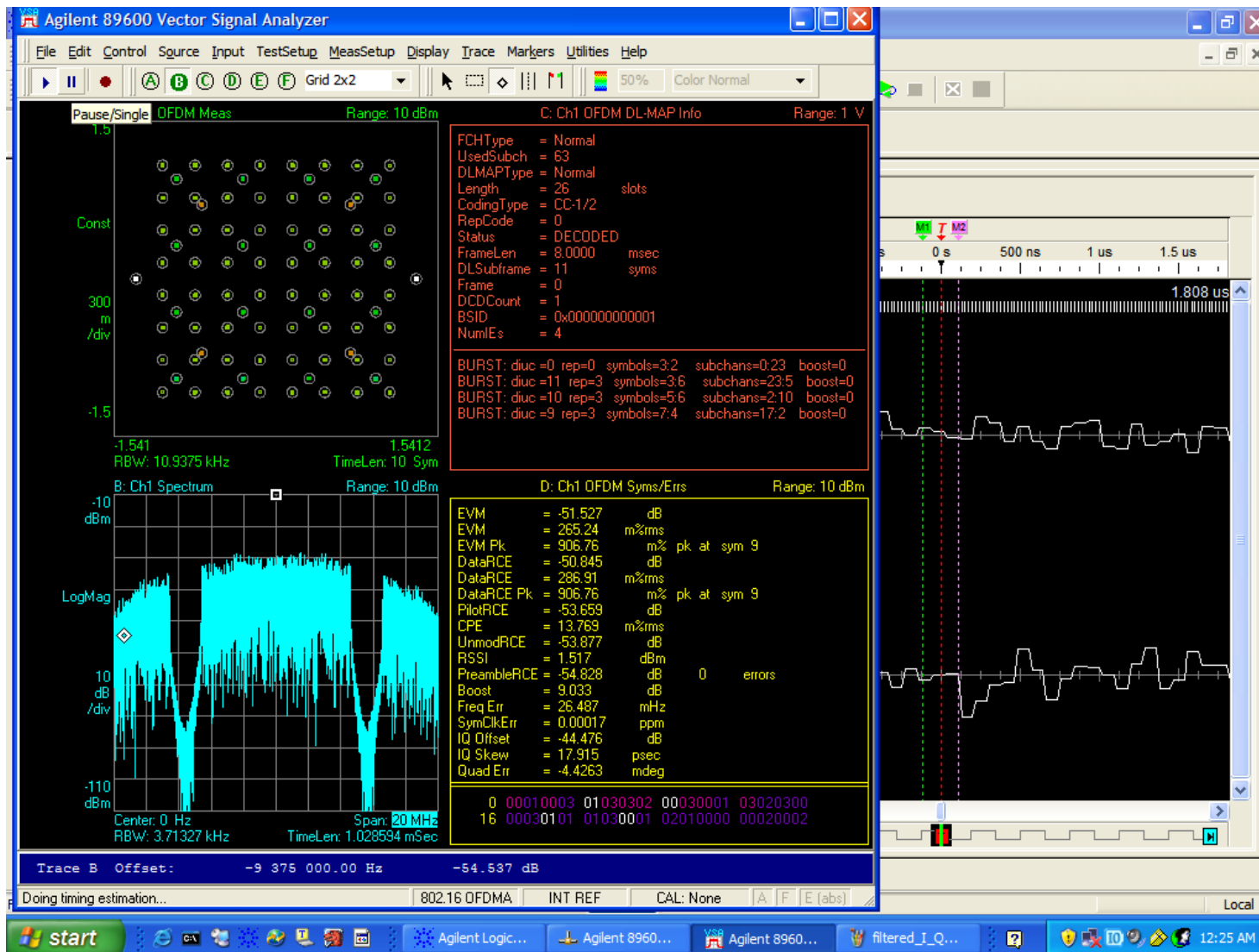
16822A logic  
analyzer (L)

MSO9404A  
oscilloscope (R)

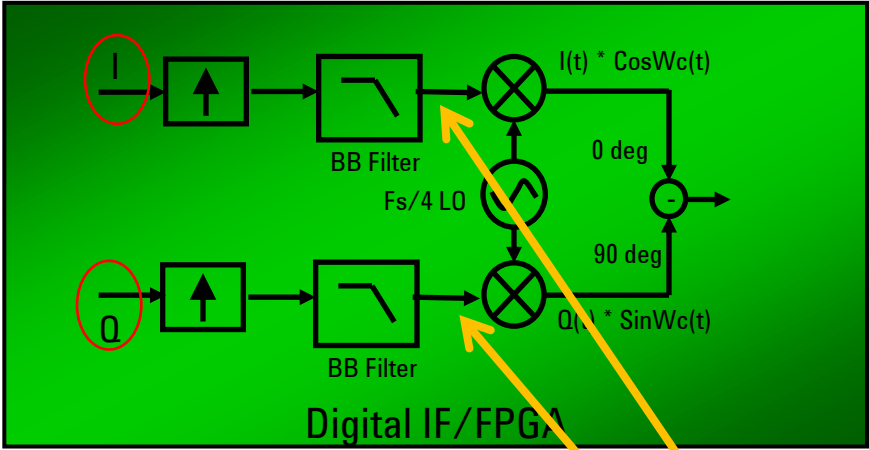
# Logic Analyzer FPGA Dynamic Probe Test Results



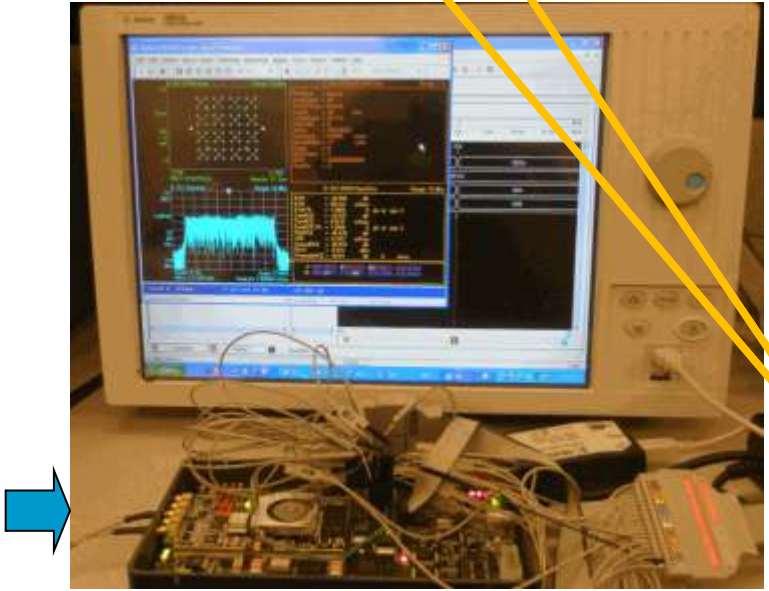
# Unfiltered I/Q fed to VSA



# Probe Filtered I and Q Data with Dynamic Probe



Use Dynamic Probe to Probe FPGA Waveform at Various Stages of the FPGA Implementation



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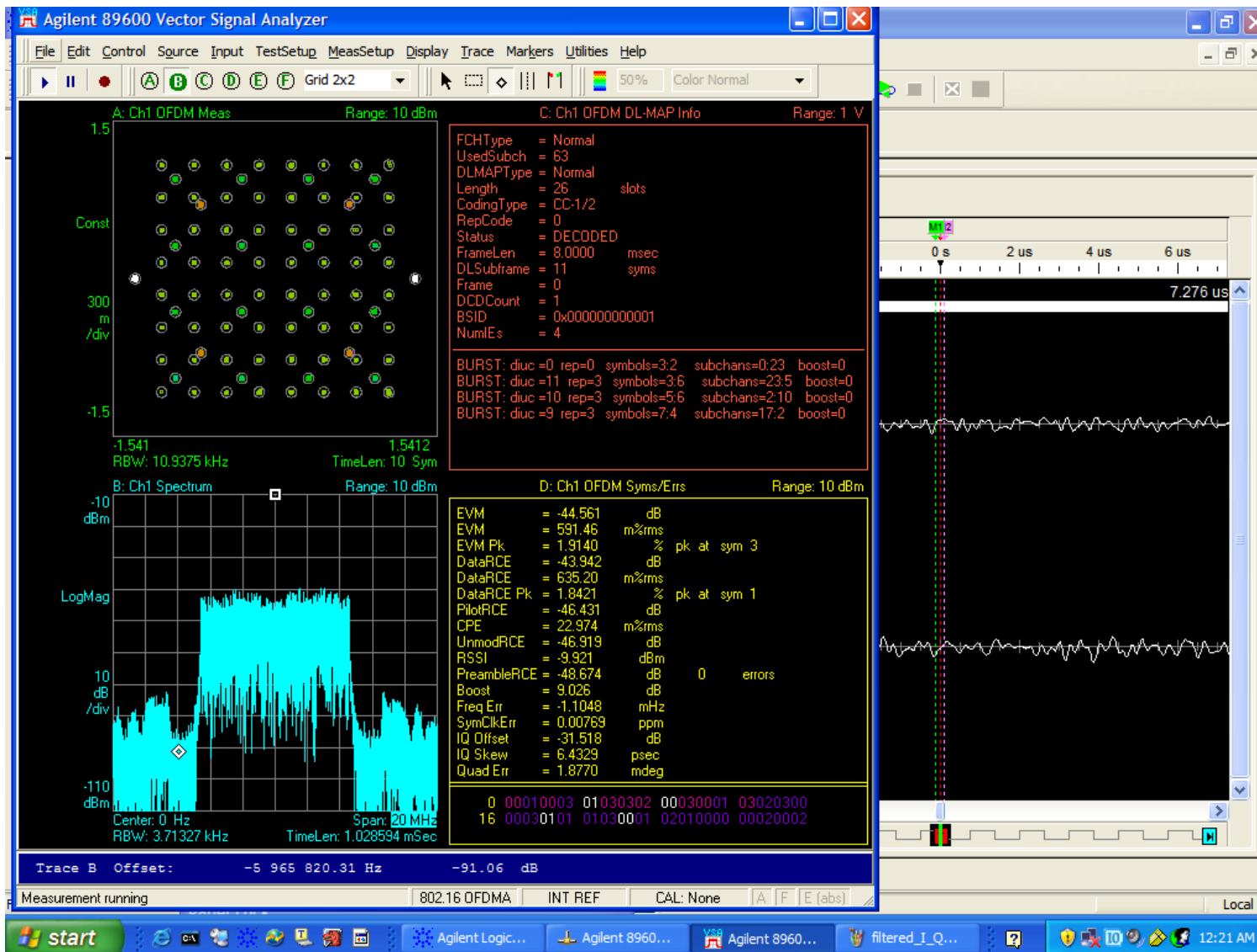
FPGA Dynamic Probe Bank Selection

Core 0

- Core 0
  - IQ\_LUT\_Outputs\_1X
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  - FIR\_Outputs\_4X
  - DAC\_Inputs\_4X**
  - Test Bank



# Filtered I/Q fed to VSA



# Summary

Re-configurable mixed-signal designs can present system-level integration testing challenges

VSA software used with simulation, logic analyzer, digital oscilloscope or PXA signal analyzer helps to isolate and debug issues

Logic analyzer dynamic probe adds another level of FPGA debugging capability to isolate digital baseband problems

# Helpful resources

16800 series logic analyzers: [www.agilent.com/find/logic](http://www.agilent.com/find/logic)

Agilent Radar Measurements Application Note:

<http://cp.literature.agilent.com/litweb/pdf/5989-7575EN.pdf>

Mixed-Signal Integration Challenges in Complex Radar Systems

<http://cp.literature.agilent.com/litweb/pdf/5990-8556EN.pdf>

Infiniium 9000 series oscilloscopes: [www.agilent.com/find/9000](http://www.agilent.com/find/9000)

89600 VSA software: [www.agilent.com/find/VSA](http://www.agilent.com/find/VSA)

System Vue: [www.agilent.com/find/SystemVue](http://www.agilent.com/find/SystemVue)

N9030A PXA: [www.agilent.com/find/pxa](http://www.agilent.com/find/pxa)

FPGA-based radar debug video:

[www.youtube.com/playlist?list=PLC34AC0190671F9F7](http://www.youtube.com/playlist?list=PLC34AC0190671F9F7)

FPGA-based LTE debug video: [www.agilent.com/find/LTE](http://www.agilent.com/find/LTE)