Mixed Signal Testing Challenges in FPGA-based Radar Systems

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Agenda

Introduction: Why Use a Logic Analyzer and Oscilloscope?

Case Study 1: Linear FM “Chirp” Radar Example

Insertion of Baseband Test Points in the FPGA

FPGA Digital Capture with Logic Analyzer / VSA

Analog IF Capture with Oscilloscope / VSA

Case Study 2: Same Hardware Reconfigured as OFDMA Comms System

Introduction: Why use a logic analyzer and oscilloscope?

With reconfigurable radar designs, whole section is digital and must probe internal to an FPGA

Logic analyzer has capability to automate digital signal capture

Logic analyzer also has ability to export captured data into VSA for analysis

Scope can capture analog IF for export to VSA as well

Allows baseband and RF teams to have common measurement framework

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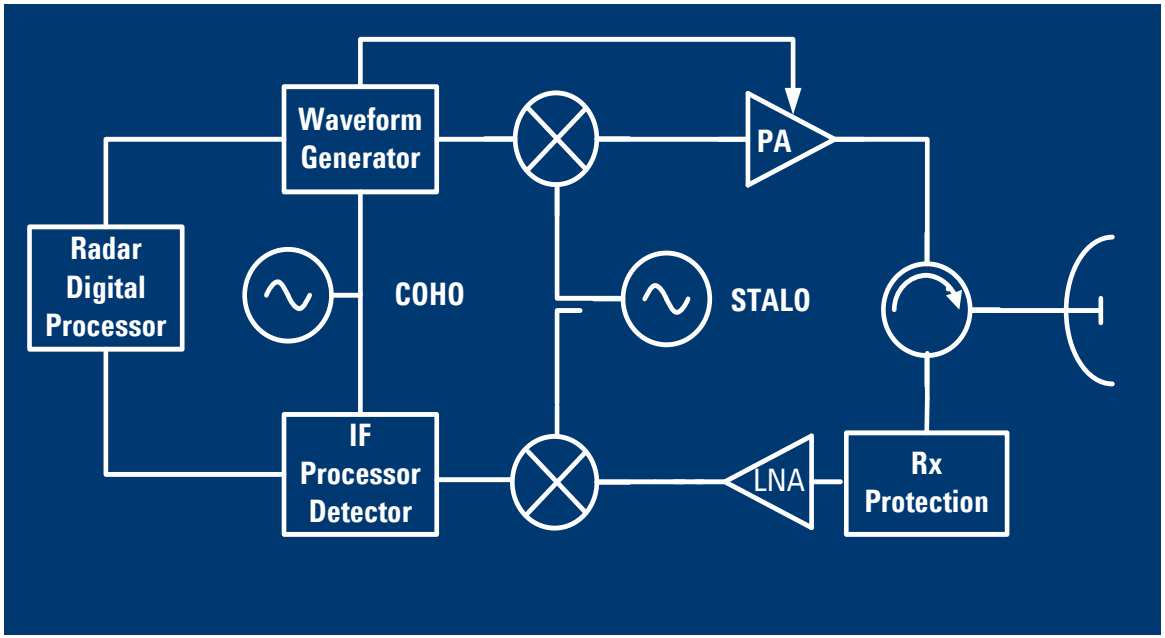
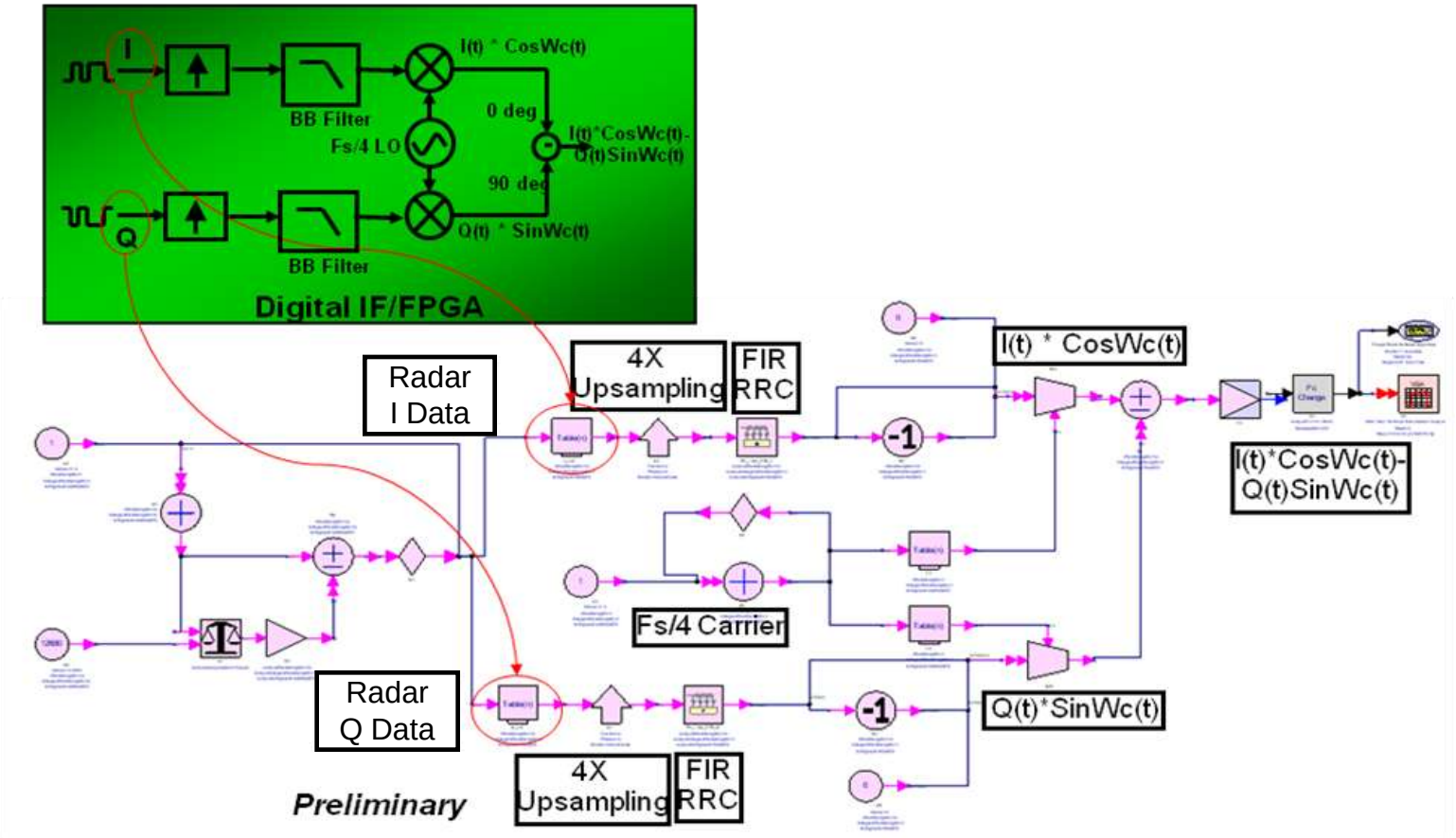
Conceptual Block Diagram
Re-Configurable Radar Subsystem

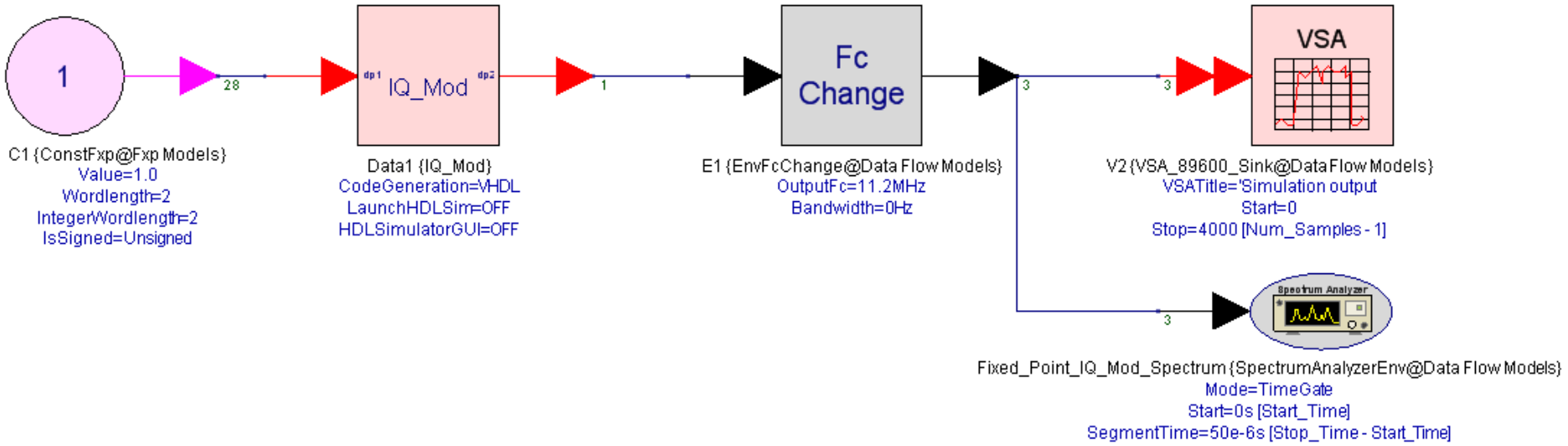


- Radar Digital Processor comprised of FPGAs and DSPs
- May be configurable for different functions
- Consider a case where it is configured as a linear FM (LFM) chirped radar
- Will show common test methodology for FPGA testing and RF testing

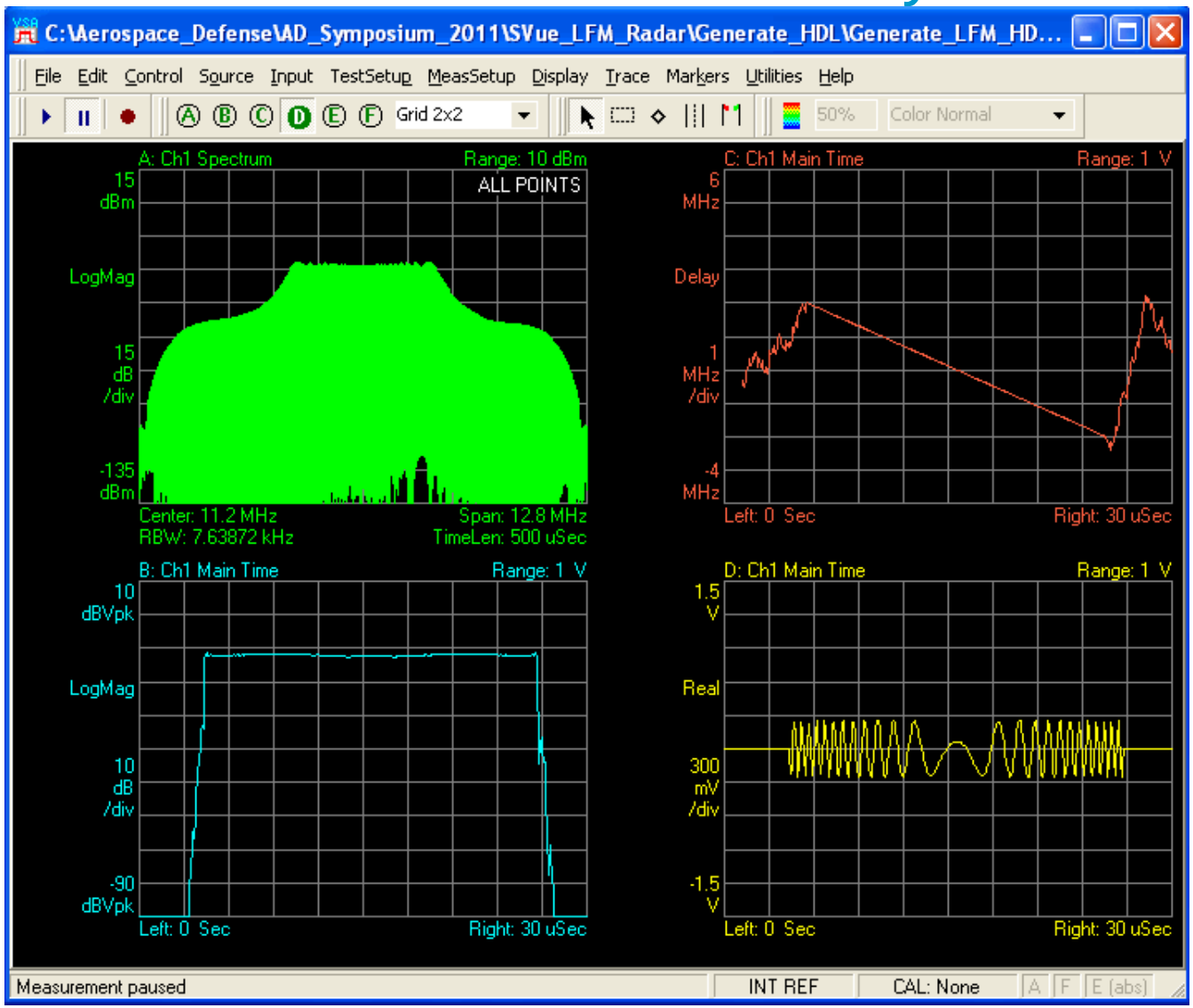
First Case Study: FPGA LFM Chirp Radar Waveform Design



Simulation in System Vue



Simulation Results in System Vue



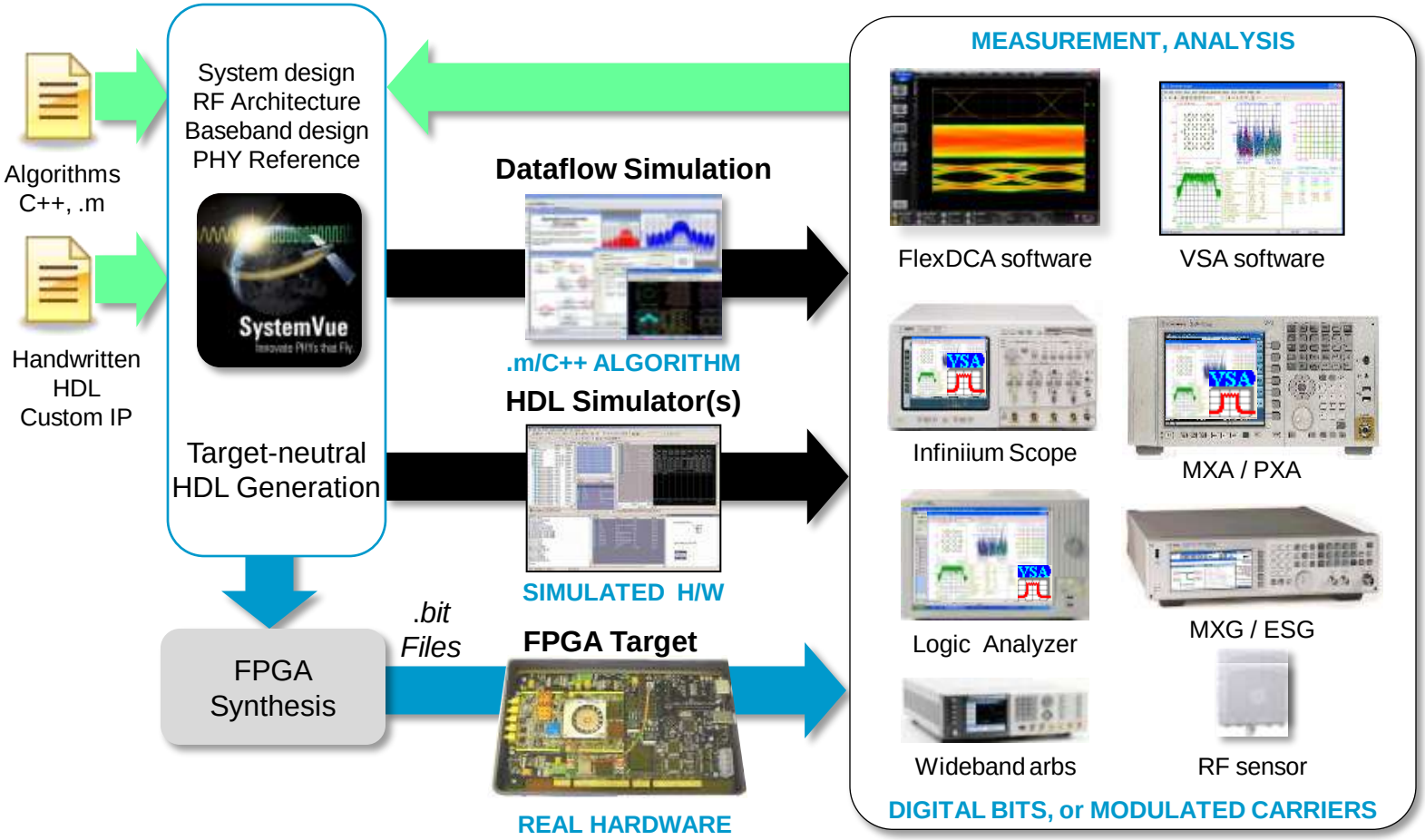
Expected spectral content

Linear frequency modulation across the pulse profile

Pulse width definition

Integrated, Tops-Down Comms ESL Flow

Cross-domain model-based design: RF, Comms, and C++/HDL



Integrated, Tops-Down Comms ESL Flow

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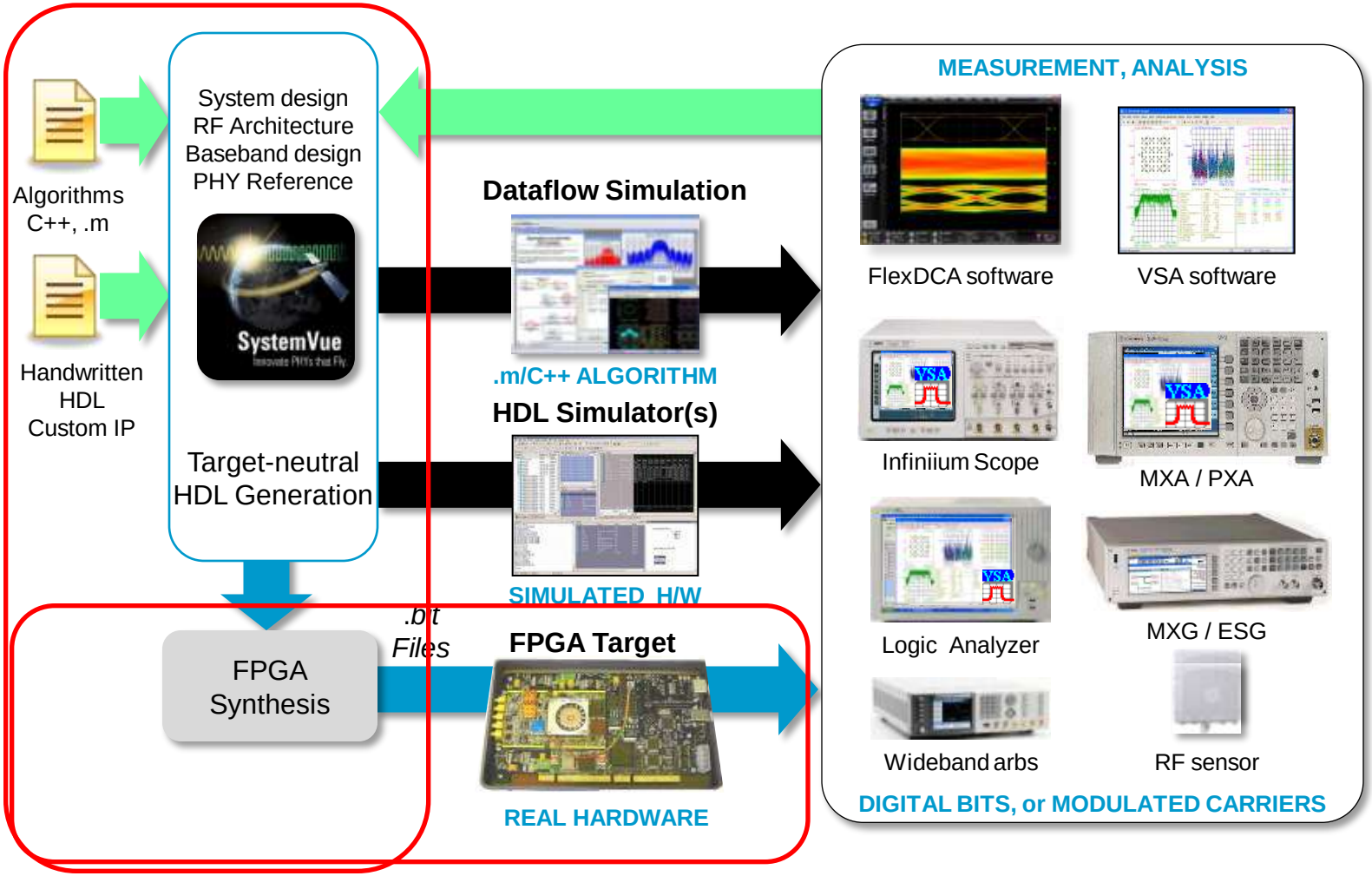

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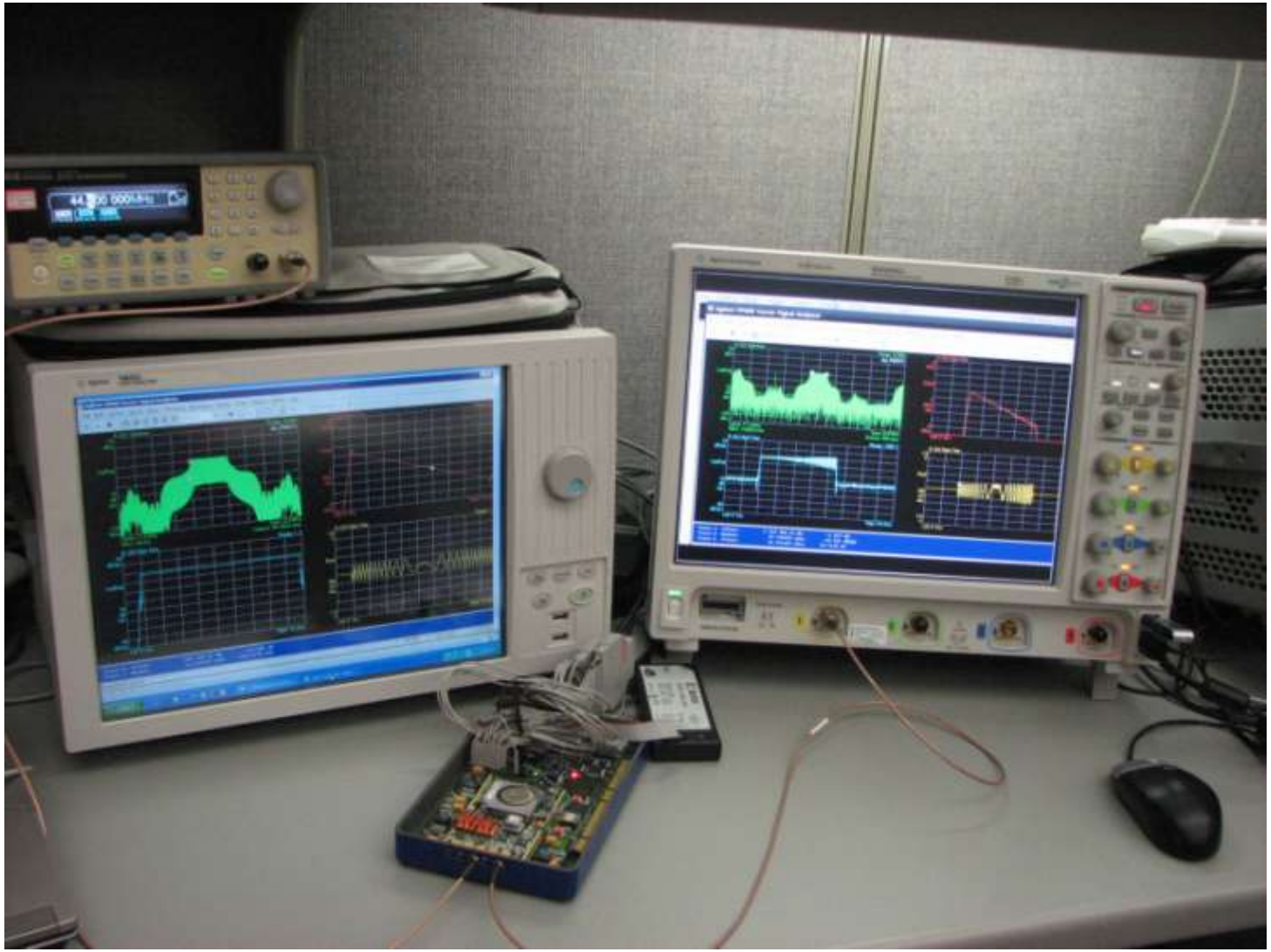
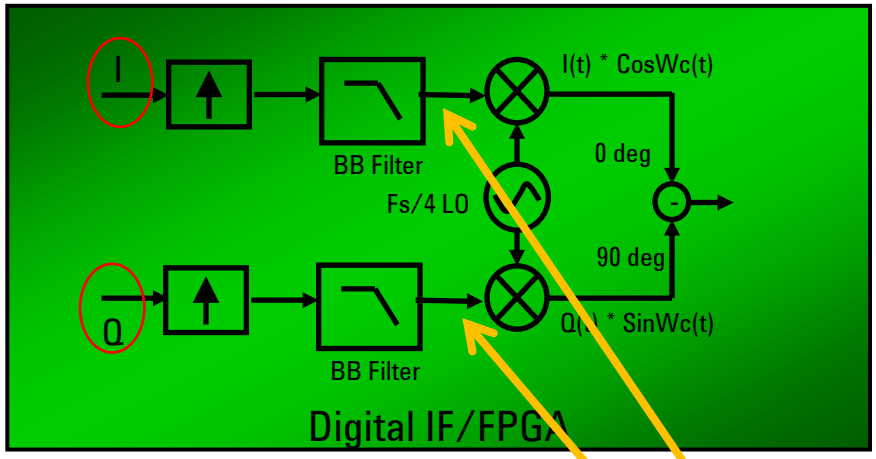
FPGA LFM Radar Test Setup



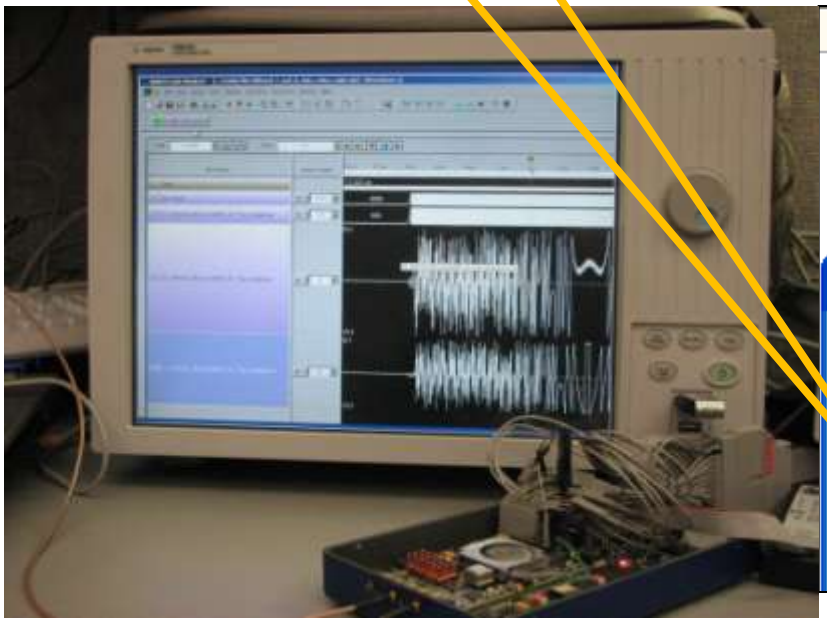
16822A logic analyzer with VSA (L)

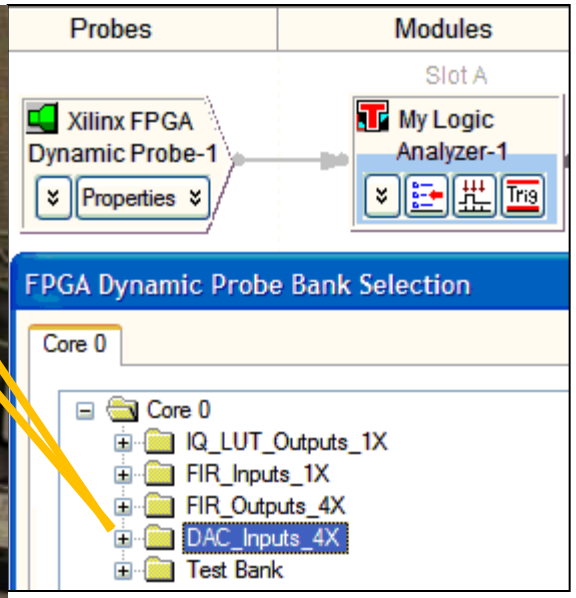
MSO9404A oscilloscope with VSA (R)

Probe Filtered I/Q in FPGA with Dynamic Probe

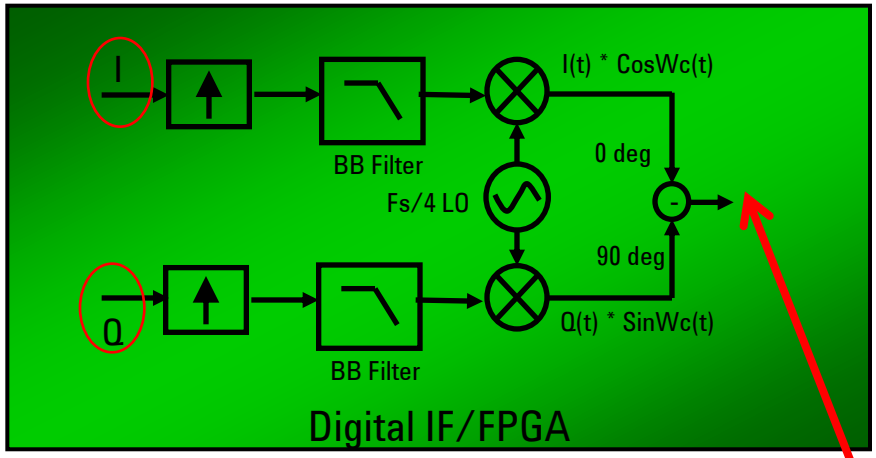


Use Dynamic Probe to Probe FPGA Waveform at Various Stages of the FPGA Implementation





Probe Digital IF in FPGA with Dynamic Probe



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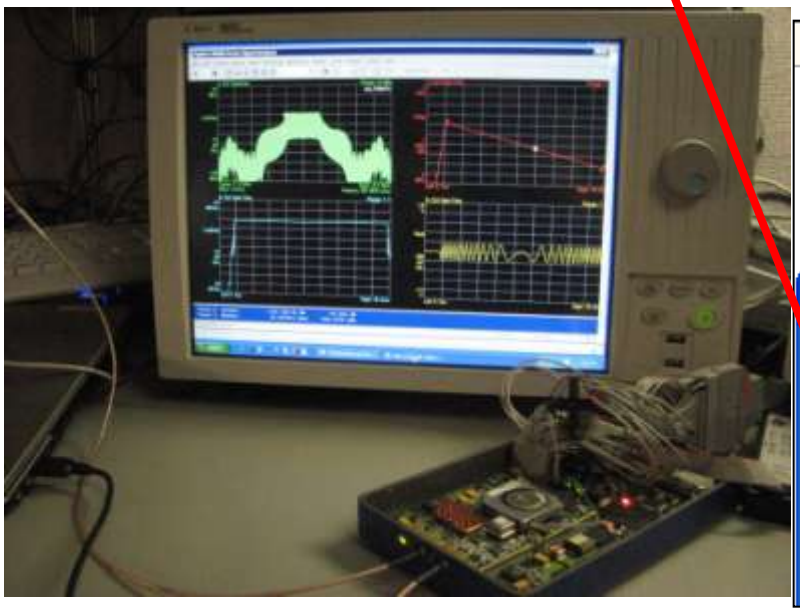
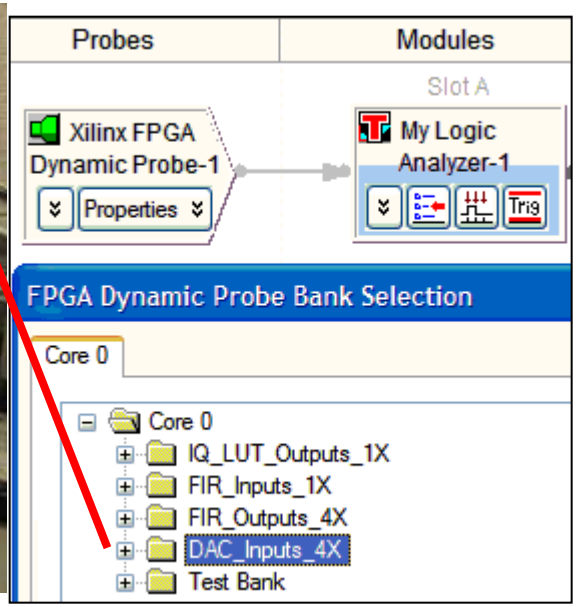
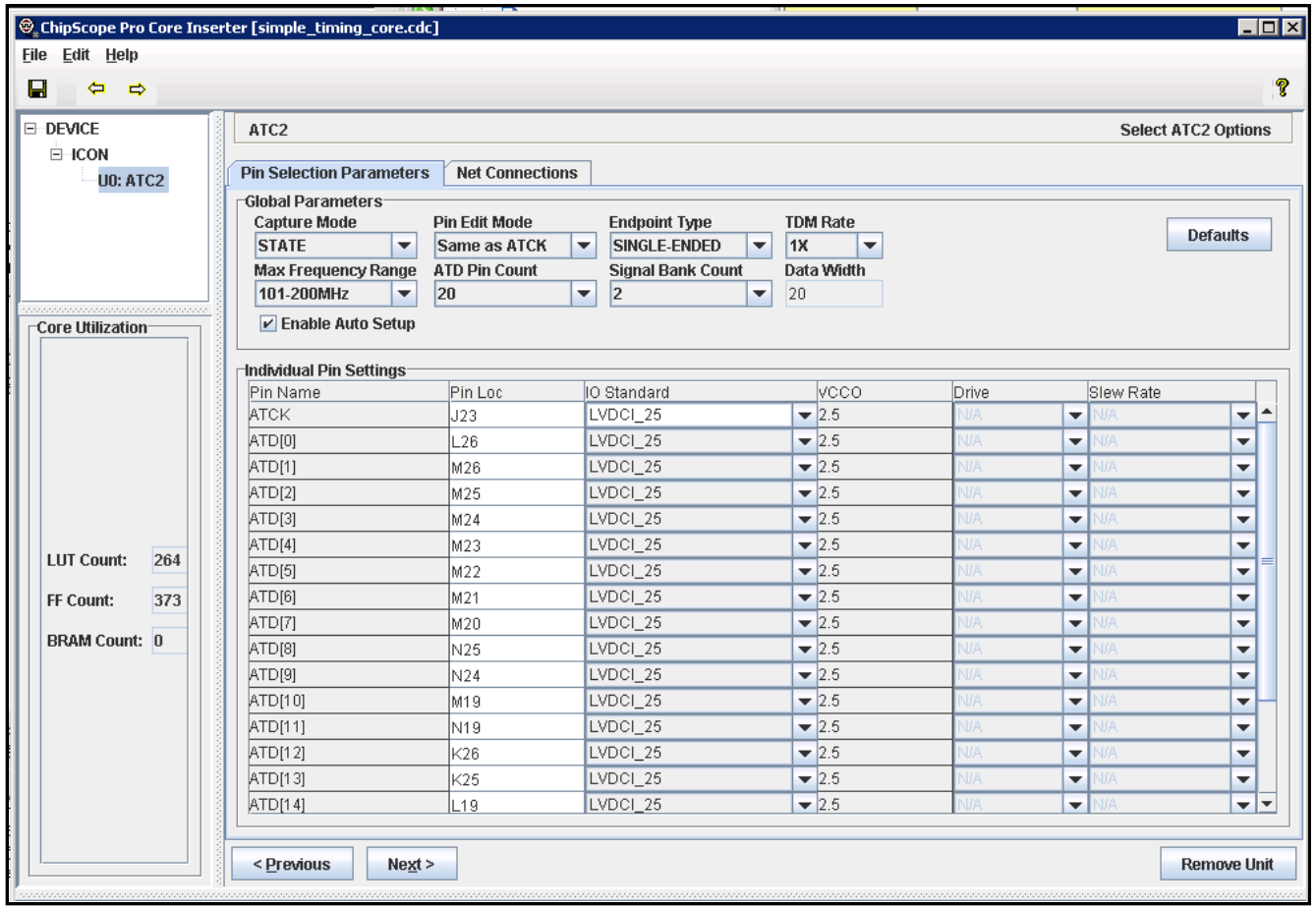


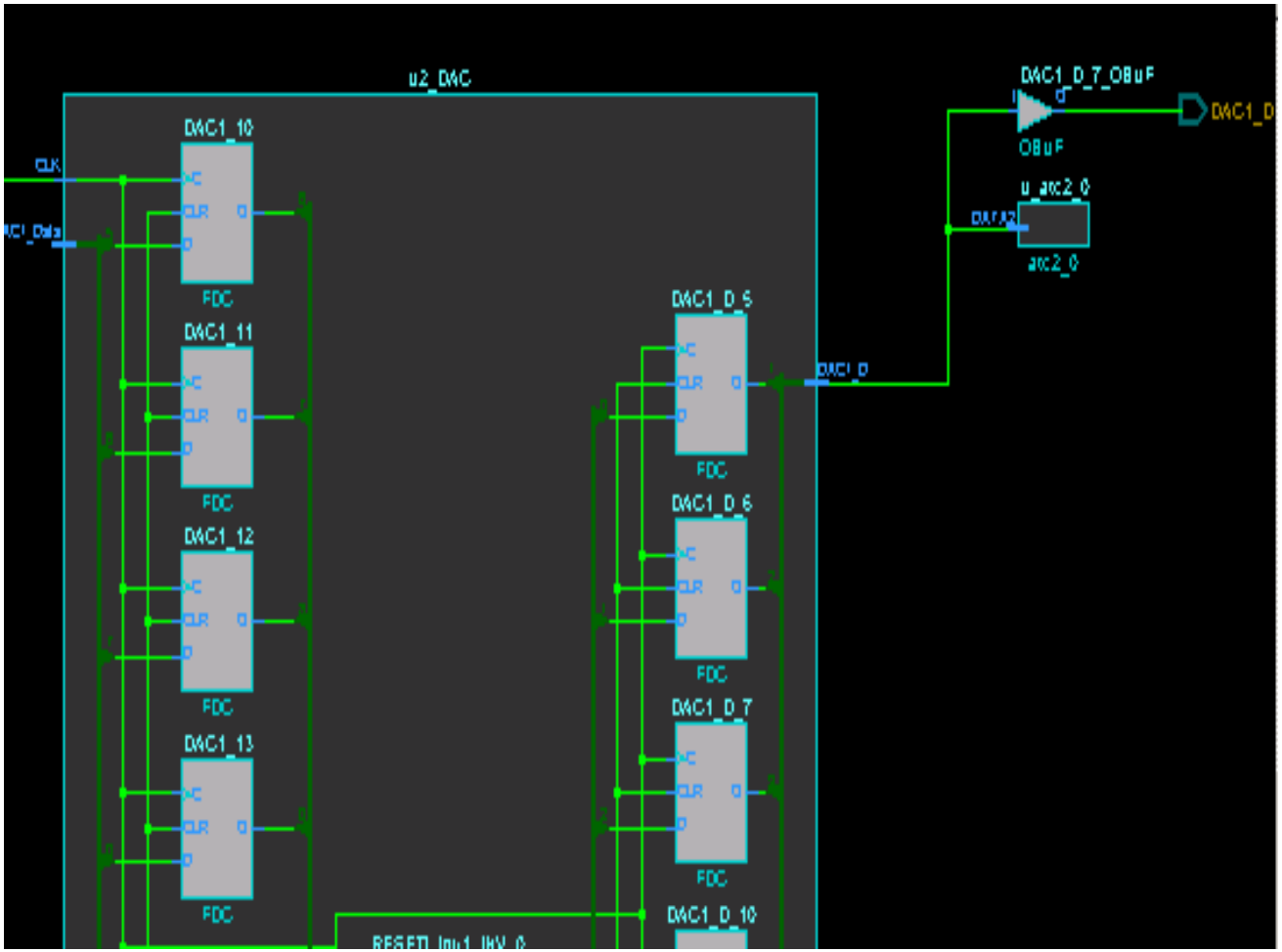


FPGA Measurement Core Configuration



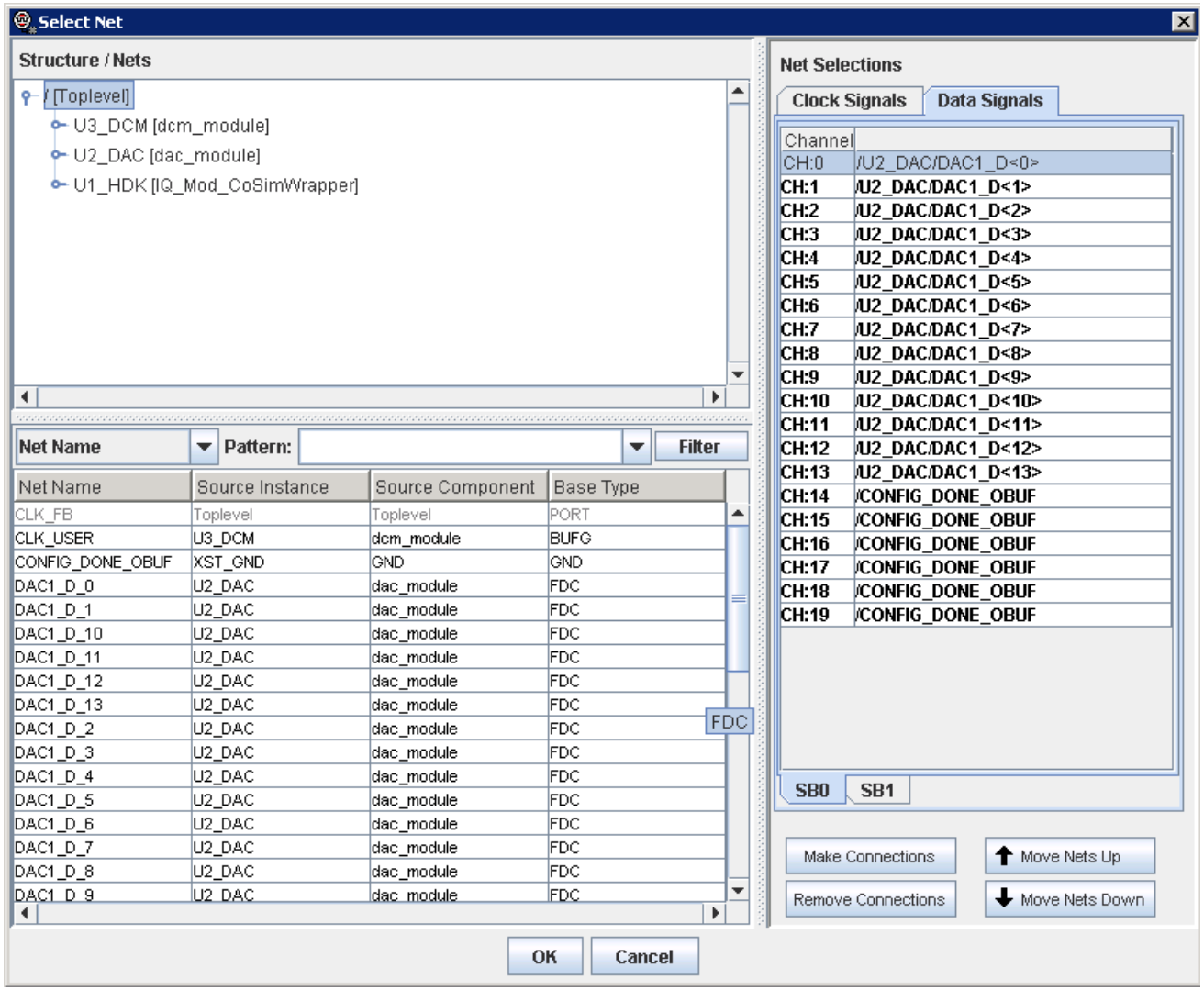
- State or timing core
- Core width
- Assign FPGA physical pins to bring out signals
- Option for time division multiplexing (2x)
- Single ended or differential output

Xilinx Plan Ahead to Assist in Net Search



- Get graphical view of FPGA implementation
- Helpful to trace signals for probing
- Here can see the bus with the digital IF signal

Assign FPGA Nets to Each Signal Bank



- Go into design hierarchy
- Select nets of interest
- "Make Connections" assigns nets to signal banks
- Also select clock signal

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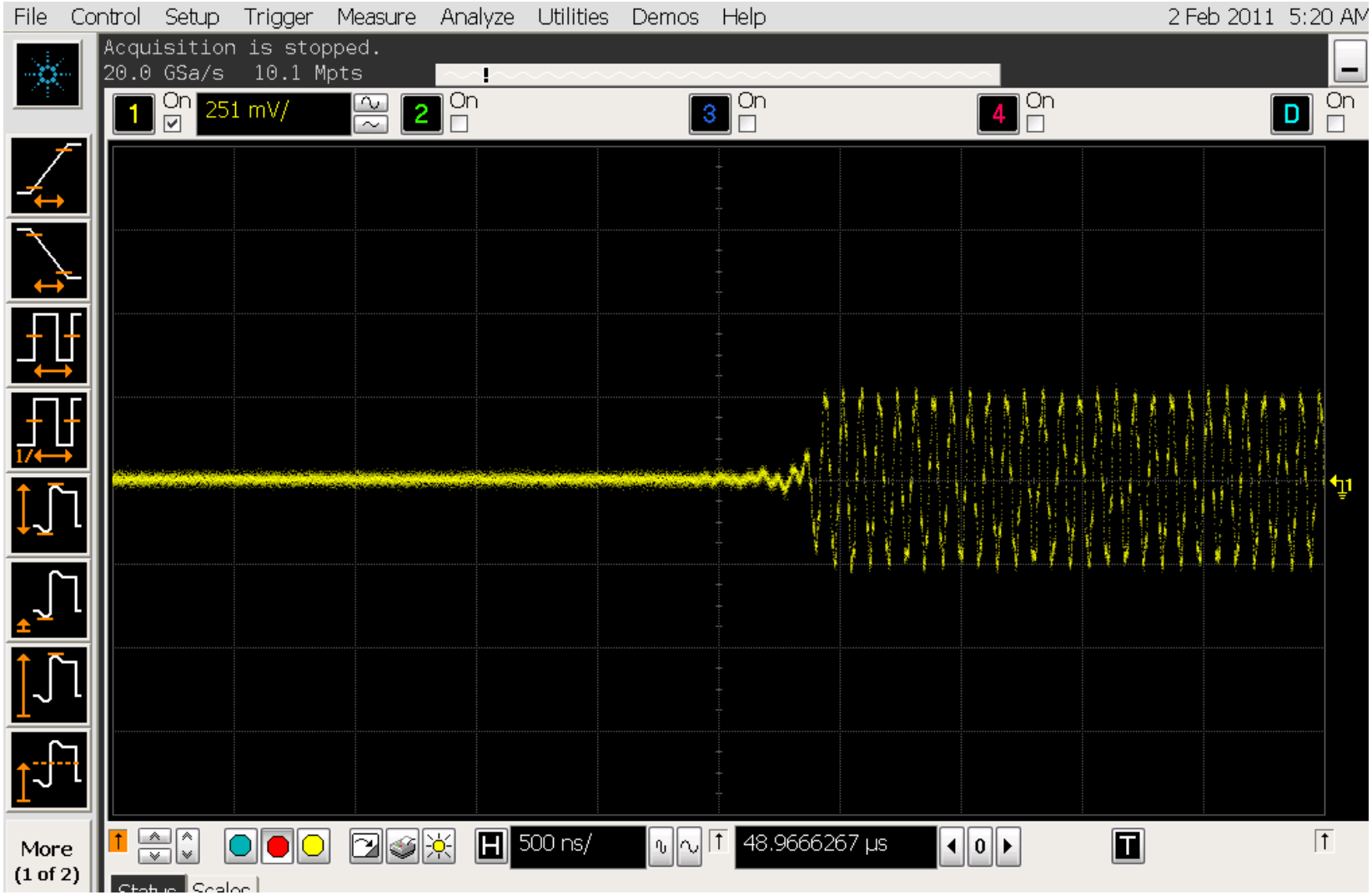
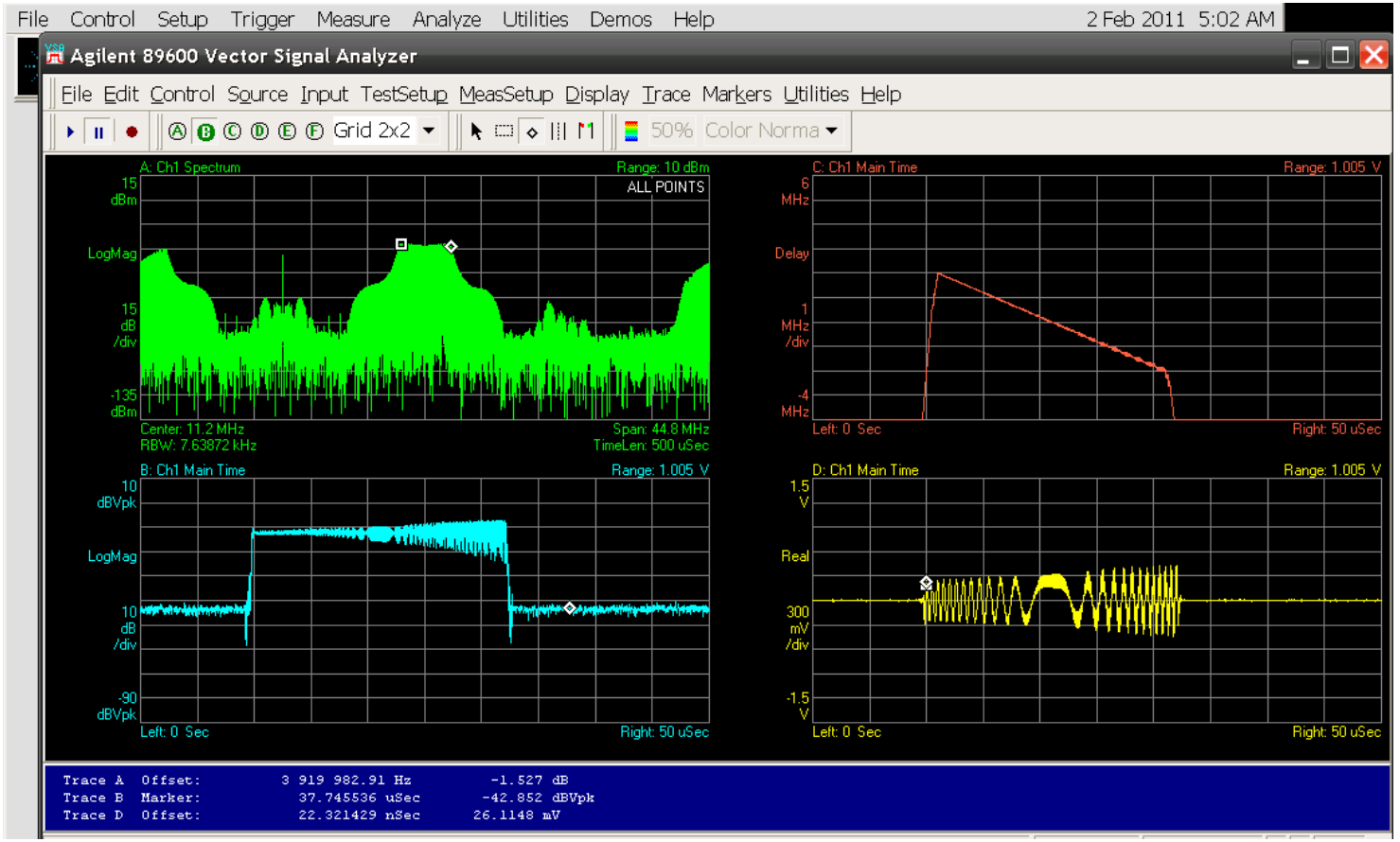
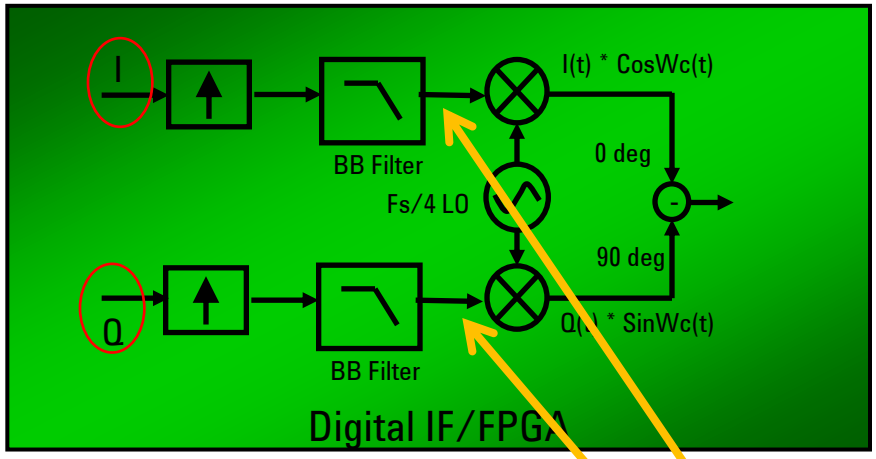
Capture FPGA LFM Radar Analog IF with Oscilloscope



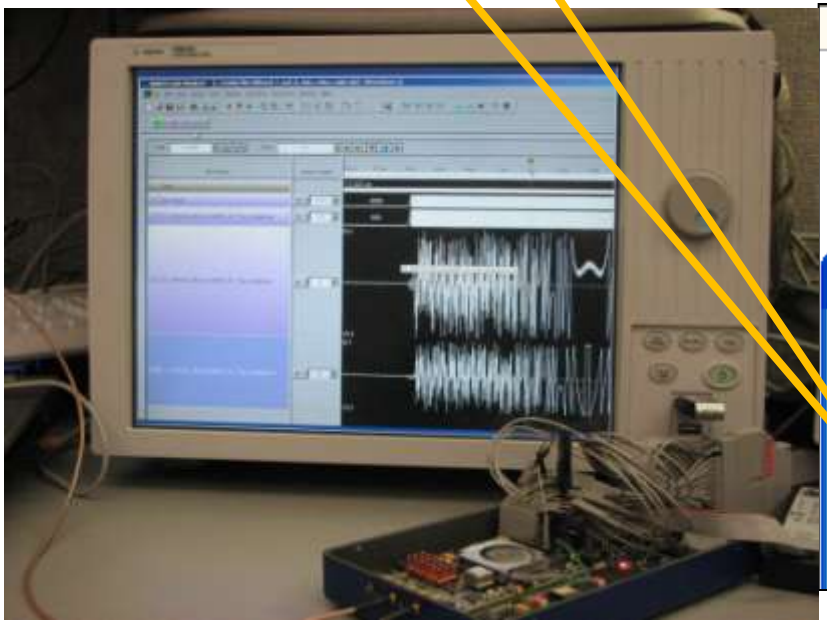
Analyze LFM Radar Analog IF with VSA Software on Oscilloscope

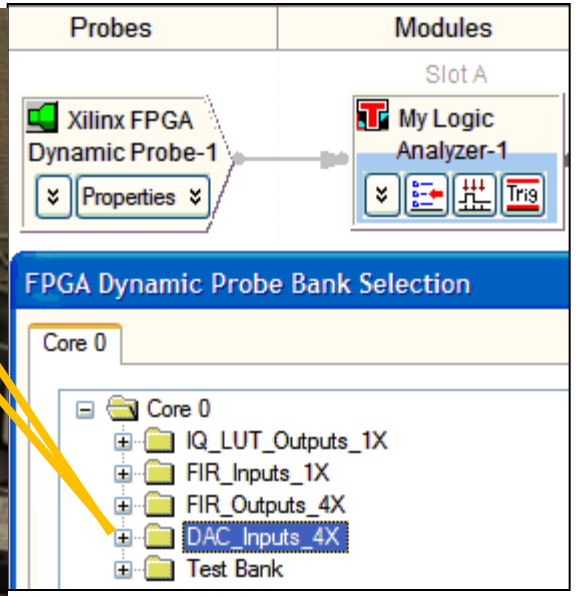


Switch to Signal Bank 1 for Filtered Digital I/Q

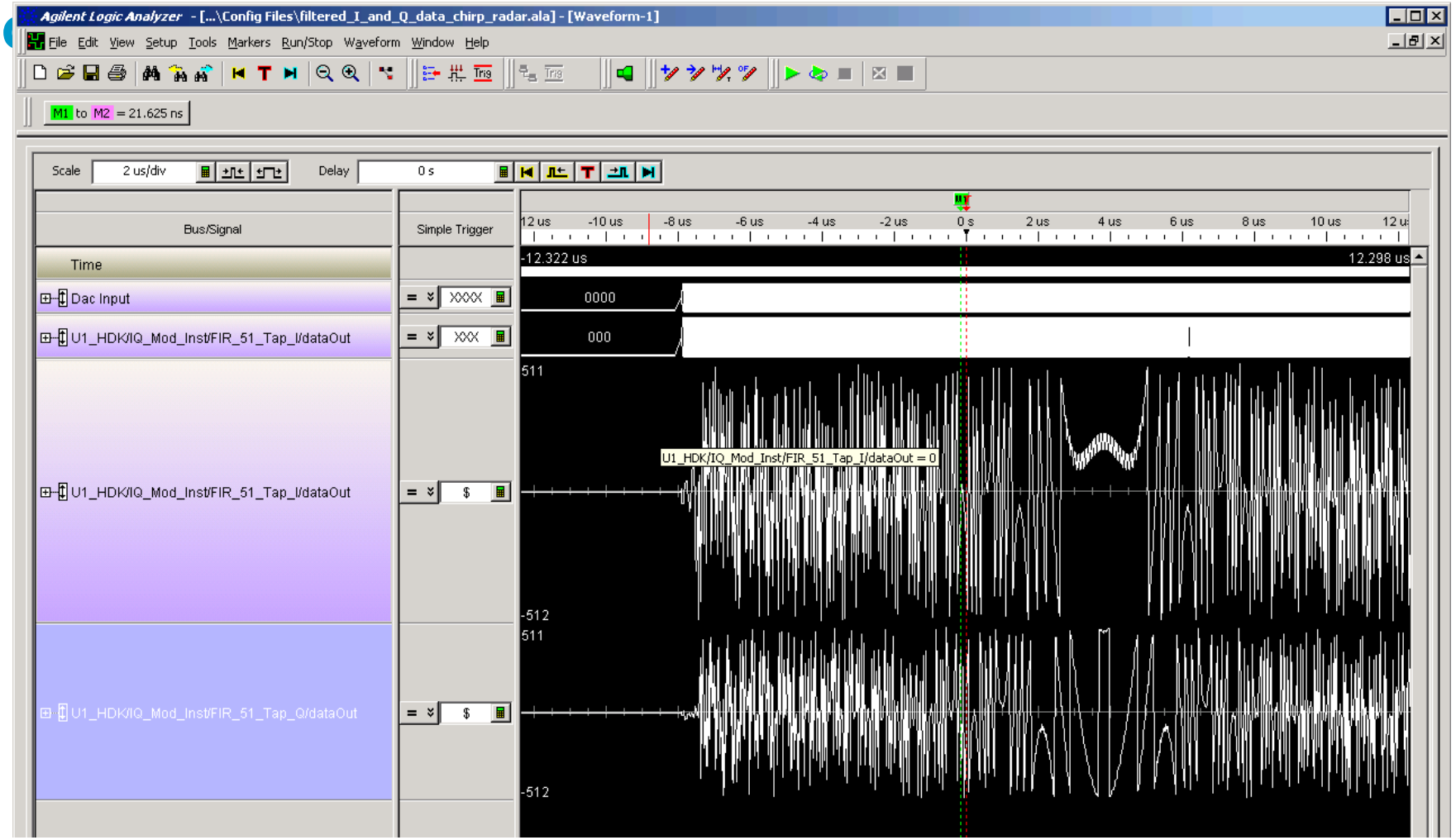


The Logic Analyzer interface allows the user to switch the FPGA MUX to move the probe points.





Capture FPGA LFM Radar Digital I/Q Waveform with L



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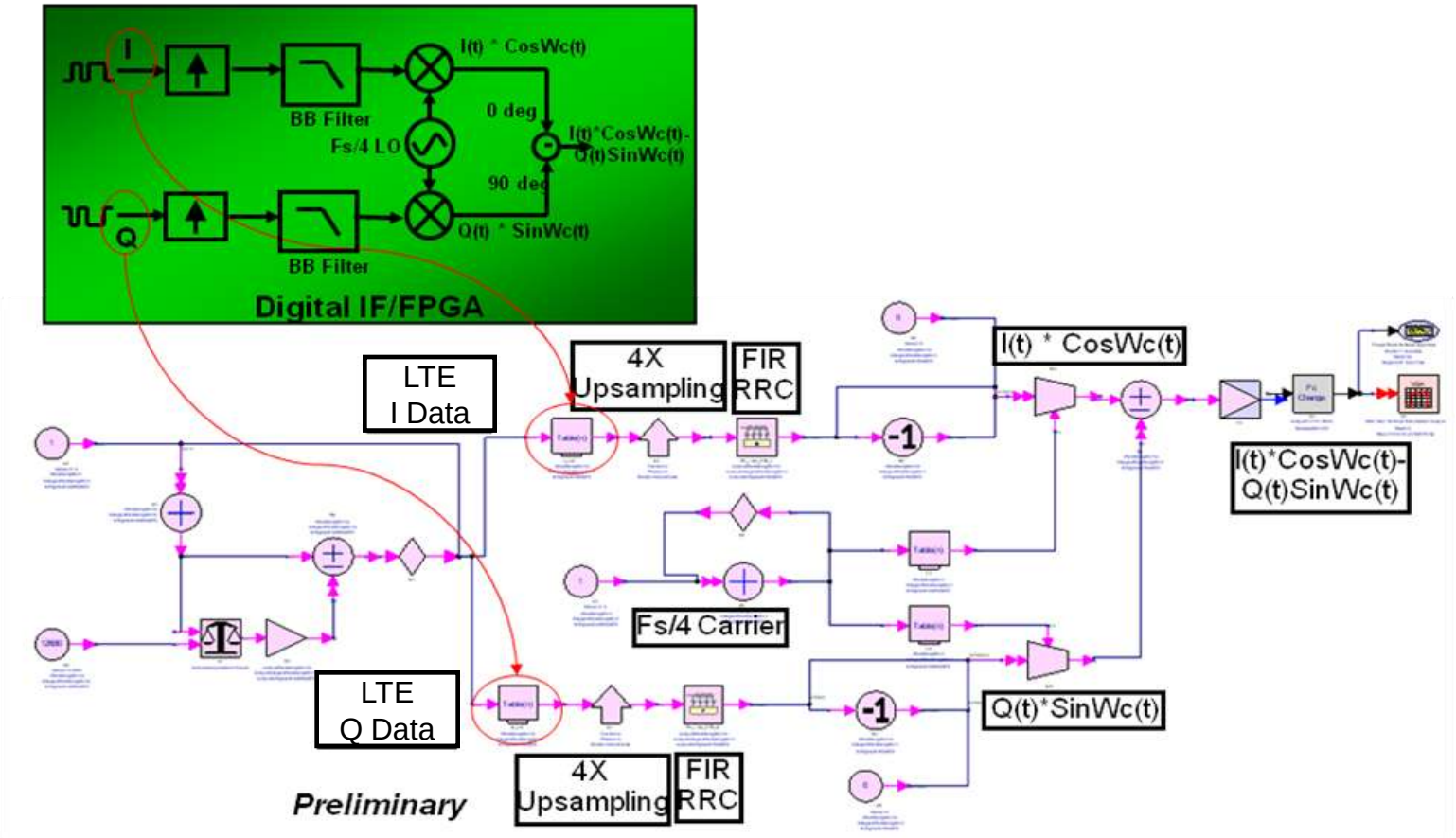
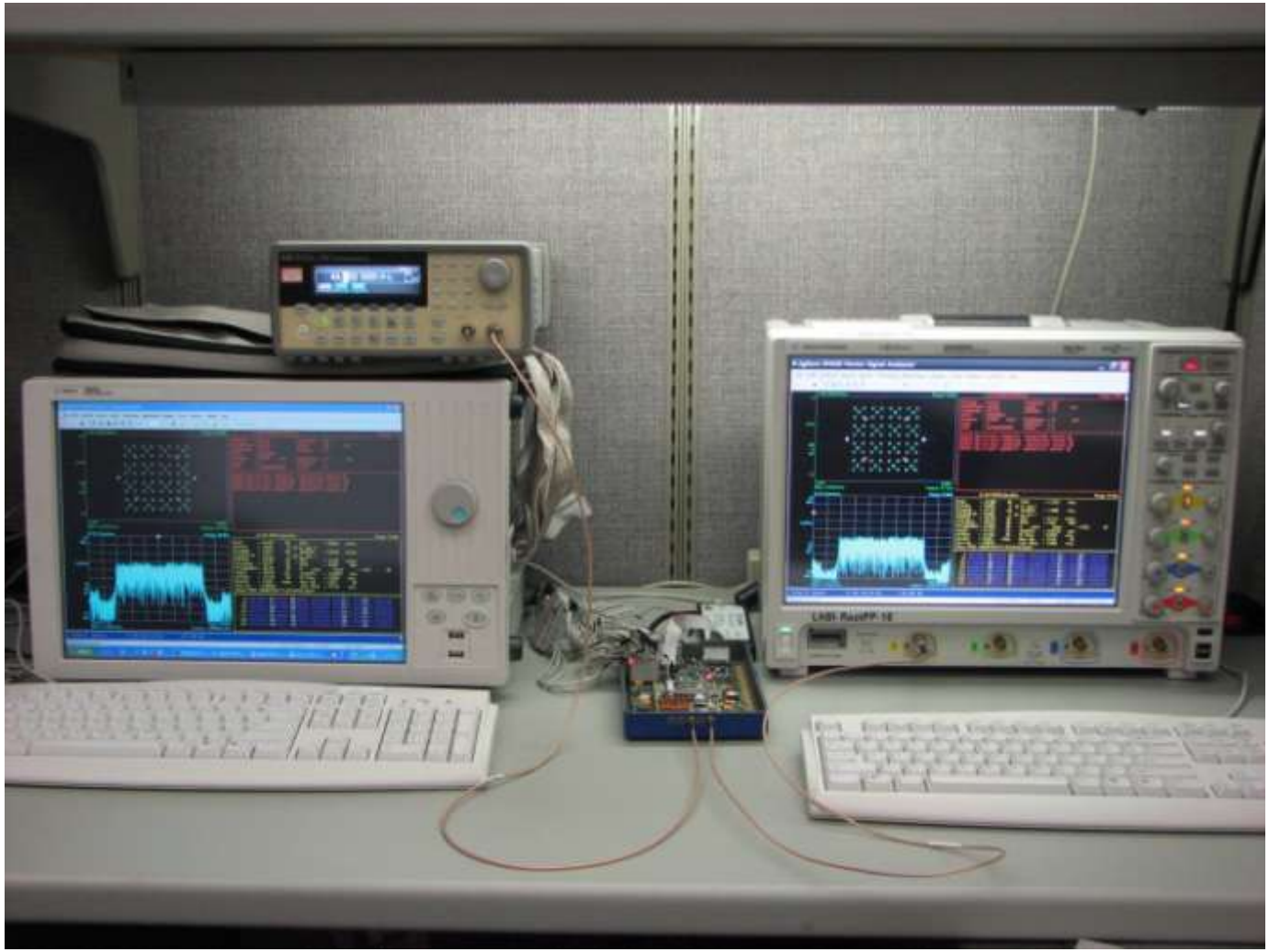
Second Case Study: FPGA Comms OFDMA Design



Second Case Study:
FPGA OFDMA Comms Test Setup



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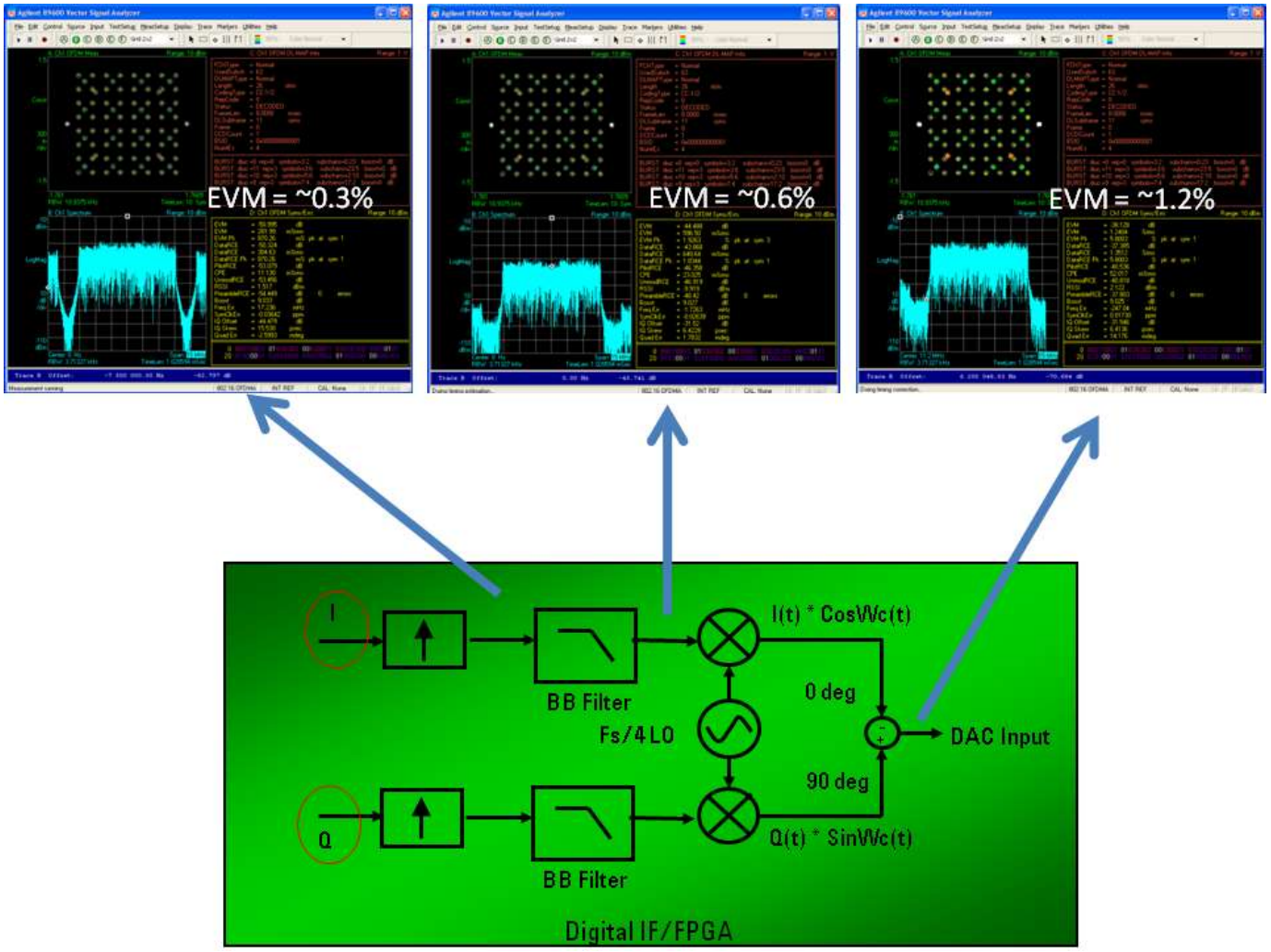
Logic Analyzer FPGA Dynamic Probe Test Results



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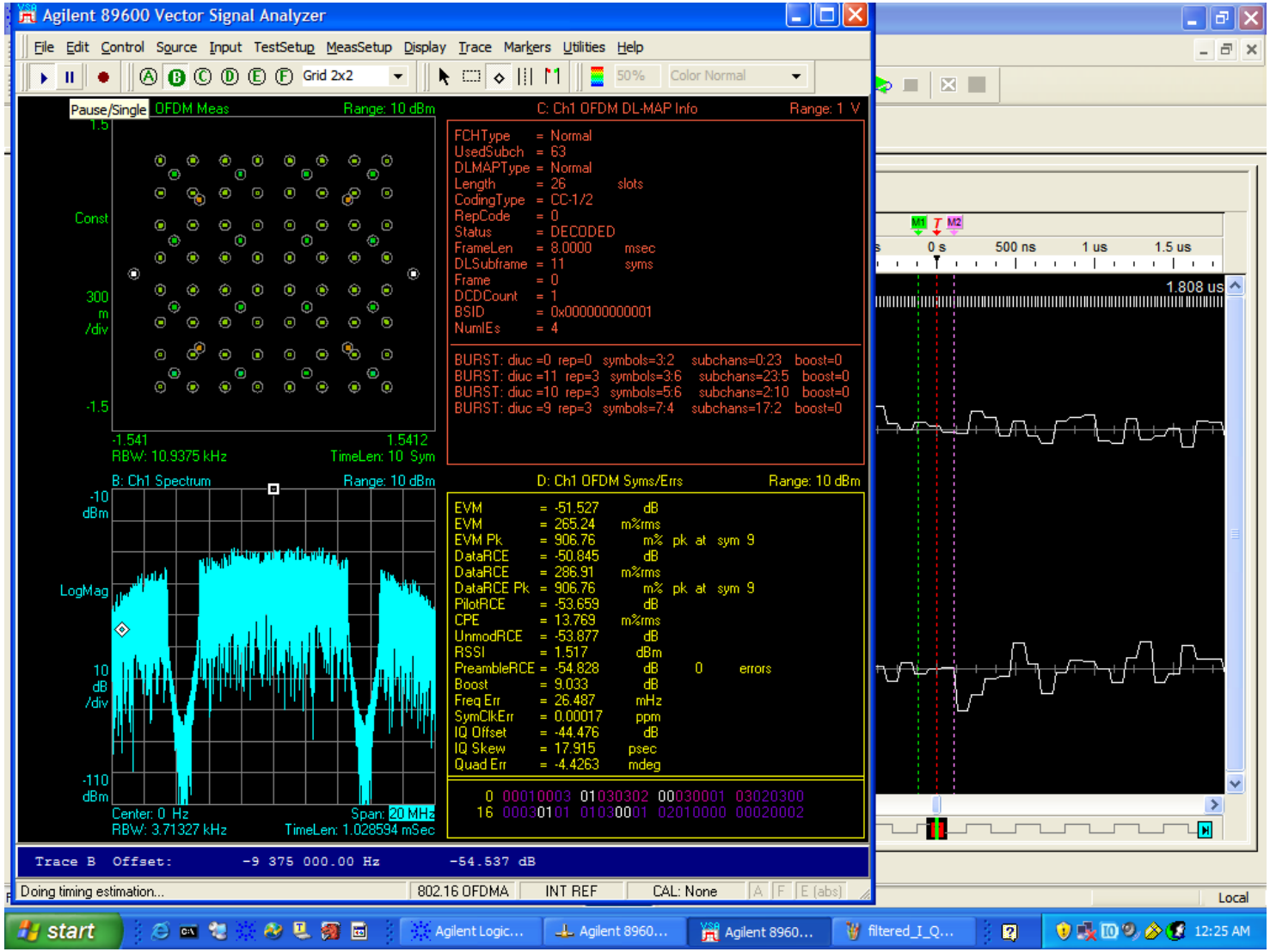
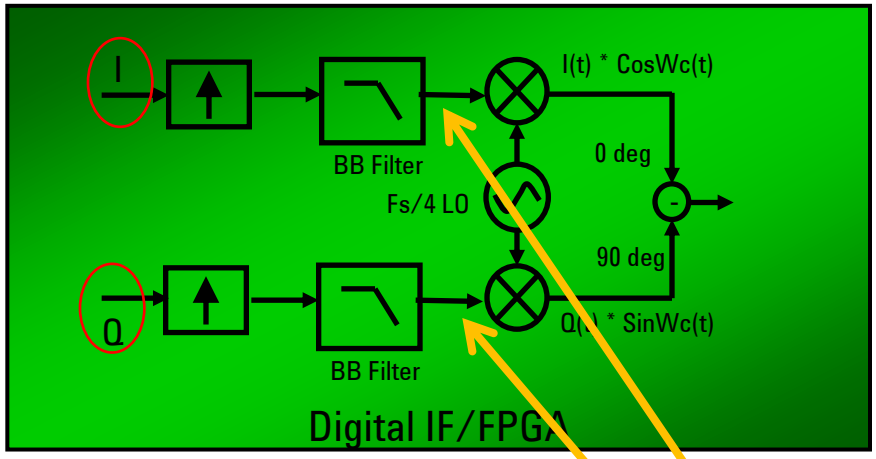
Unfiltered I/Q fed to VSA



Probe Filtered I and Q Data with Dynamic Probe



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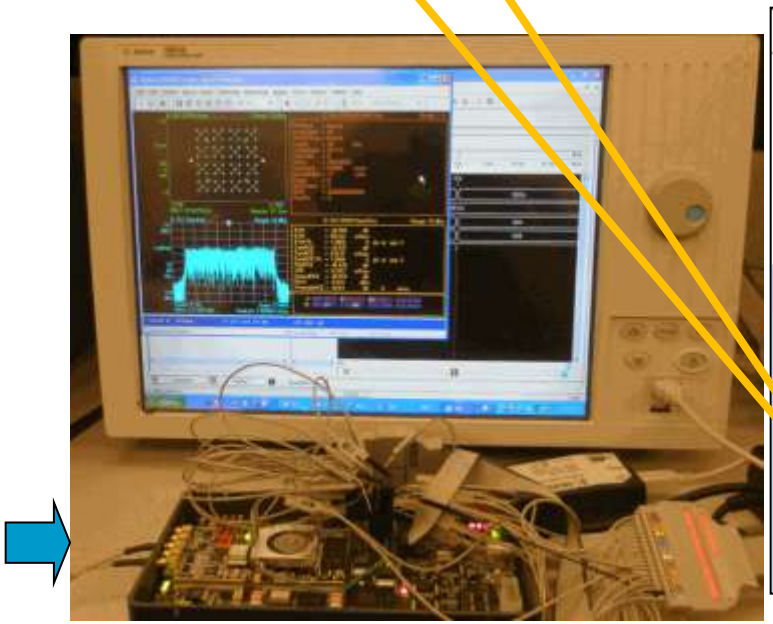
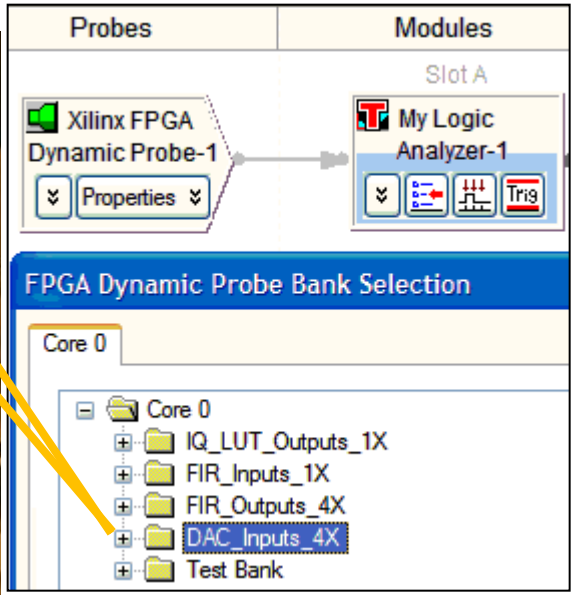
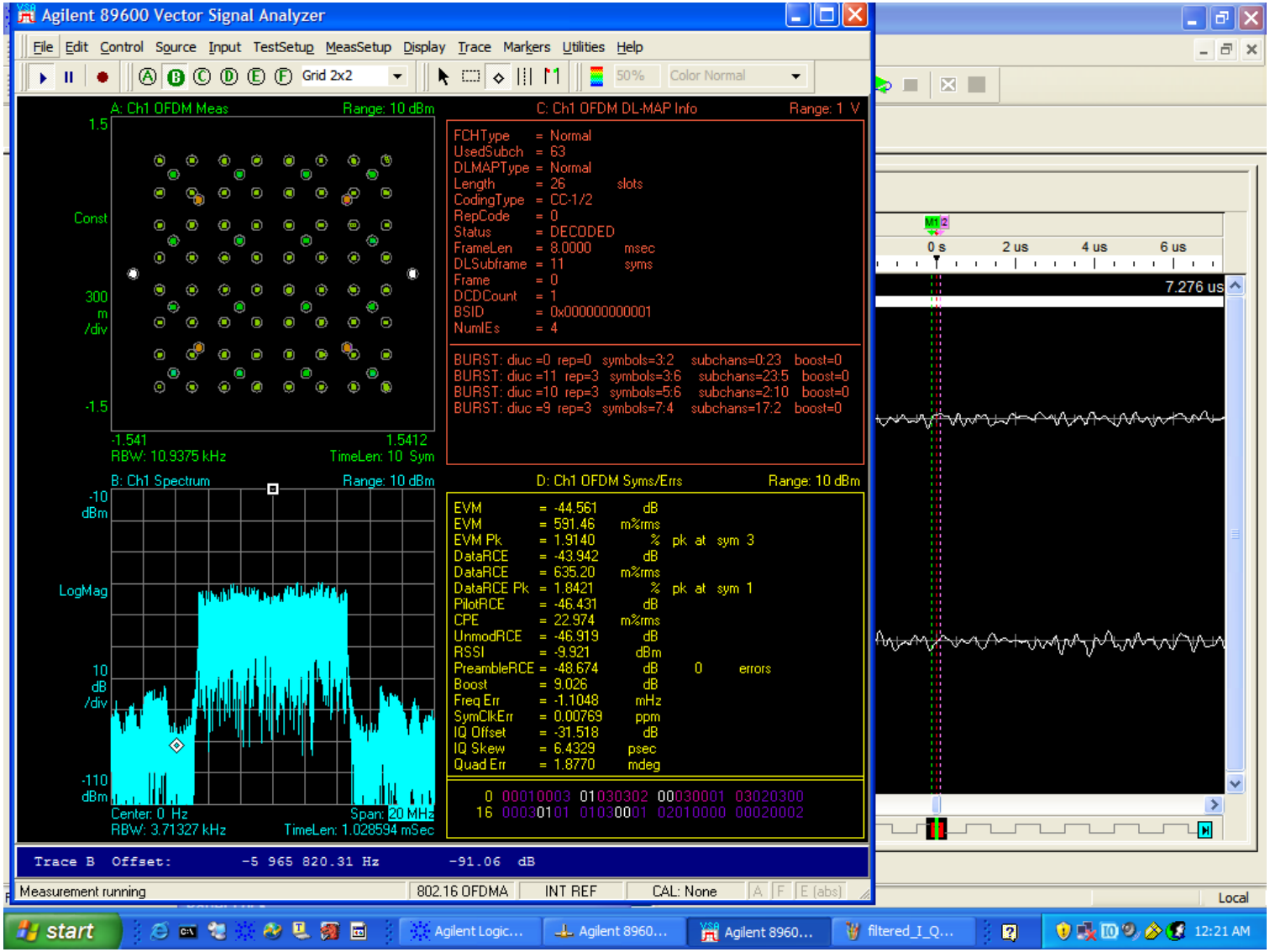




Filtered I/Q fed to VSA



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Summary

Re-configurable mixed-signal designs can present system-level integration testing challenges

VSA software used with simulation, logic analyzer, digital oscilloscope or PXA signal analyzer helps to isolate and debug issues

Logic analyzer dynamic probe adds another level of FPGA debugging capability to isolate digital baseband problems

Helpful resources

16800 series logic analyzers: www.agilent.com/find/logic

Agilent Radar Measurements Application Note:
http://cp.literature.agilent.com/litweb/pdf/5989-7575EN.pdf

Mixed-Signal Integration Challenges in Complex Radar Systems
http://cp.literature.agilent.com/litweb/pdf/5990-8556EN.pdf

Infiniium 9000 series oscilloscopes: www.agilent.com/find/9000

89600 VSA software: www.agilent.com/find/VSA

System Vue: www.agilent.com/find/SystemVue

N9030A PXA: www.agilent.com/find/pxa

FPGA-based radar debug video:
www.youtube.com/playlist?list=PLC34AC0190671F9F7

FPGA-based LTE debug video: www.agilent.com/find/LTE