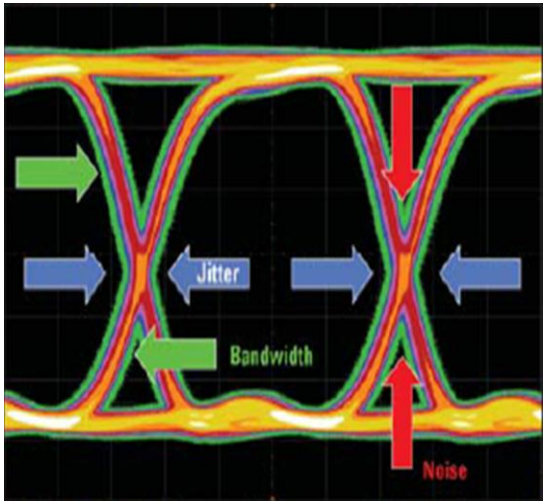
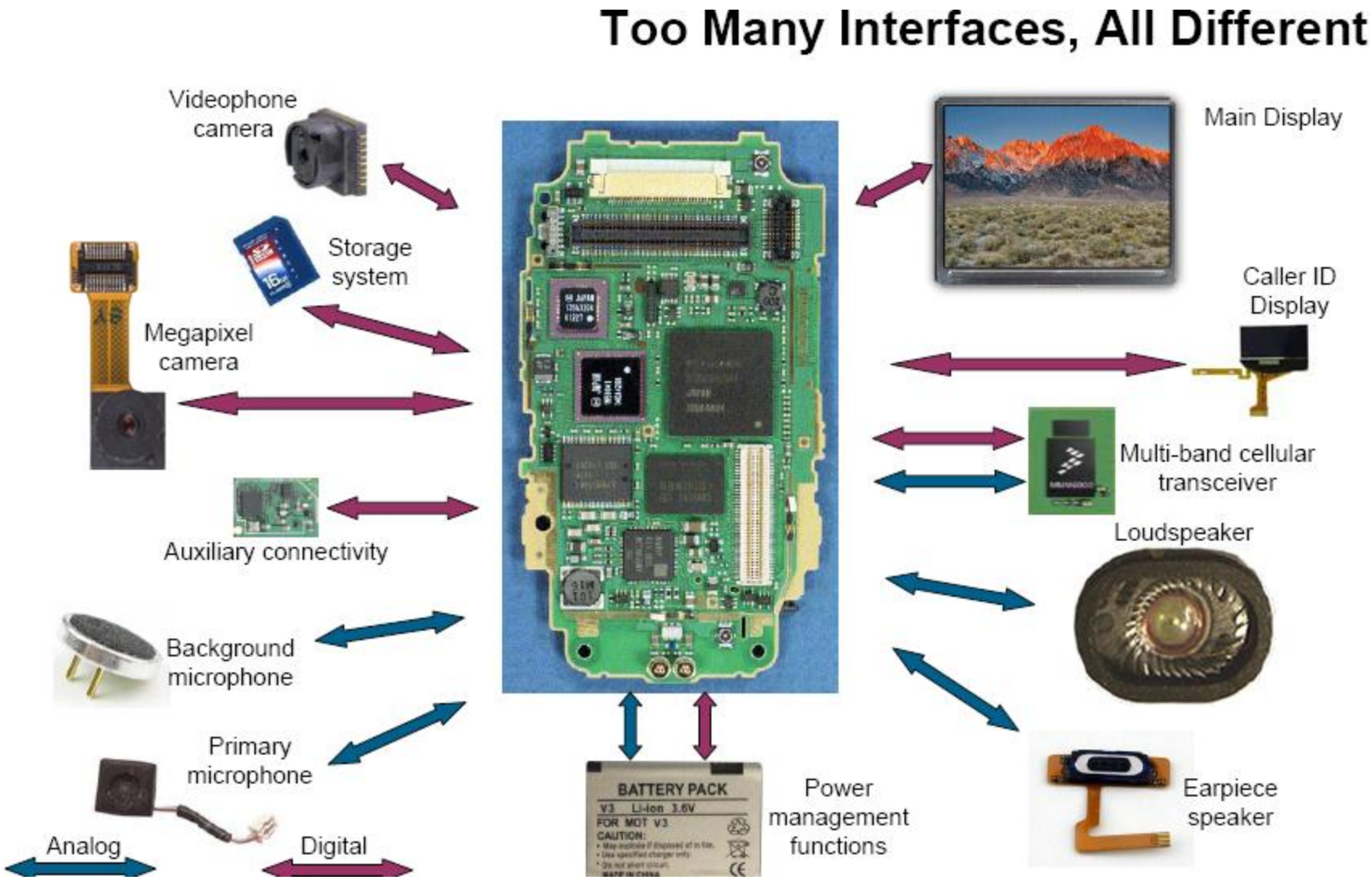
High Speed Digital Design and Validation Seminar

25/4/12



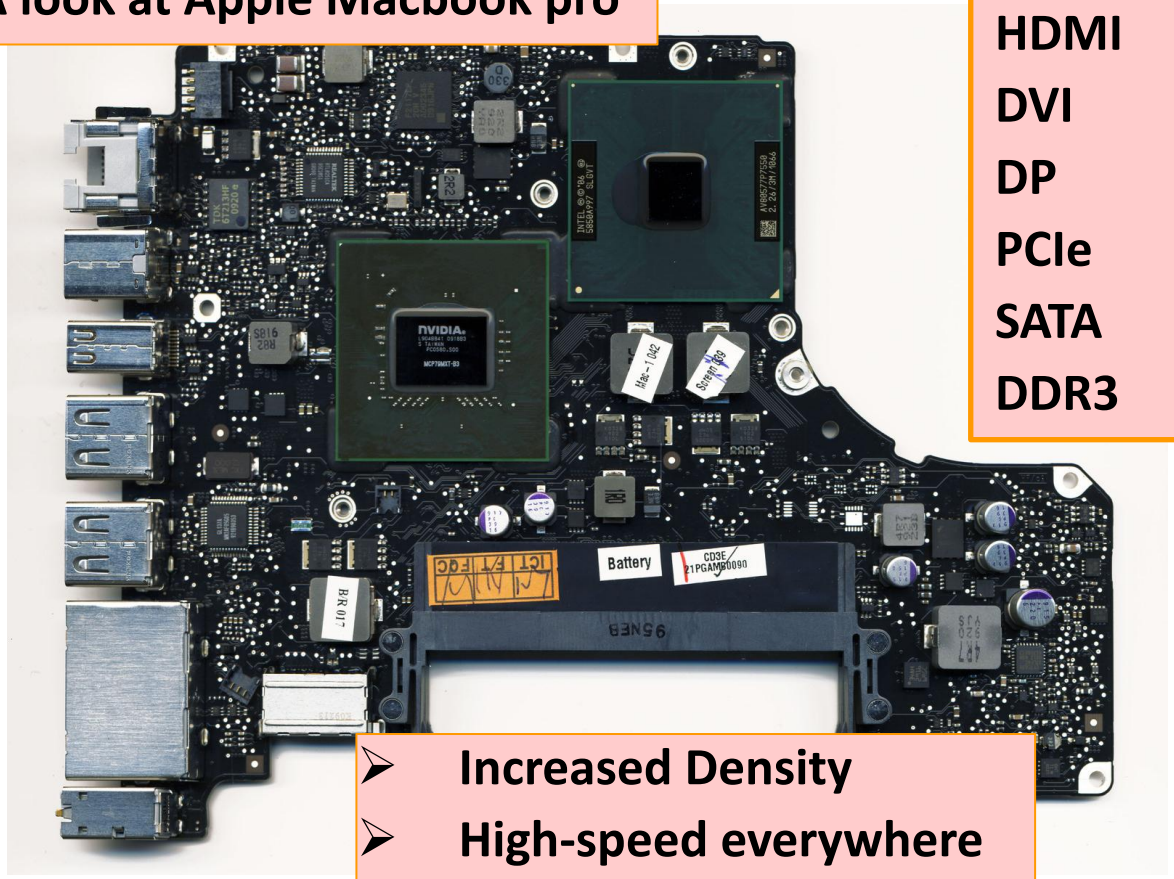
Welcome!

High Speed Digital Interfaces are Everywhere!



Chip-to-chip Interconnect goes Serial, goes fast and needs to co-exist

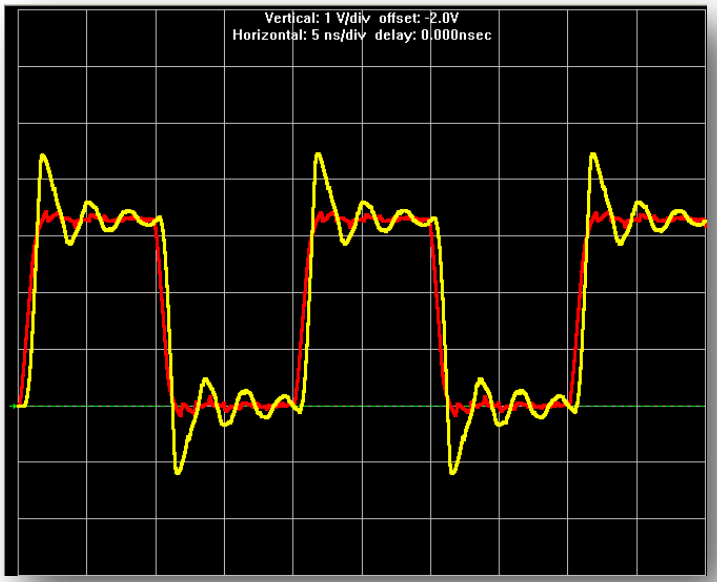
A look at Apple Macbook pro

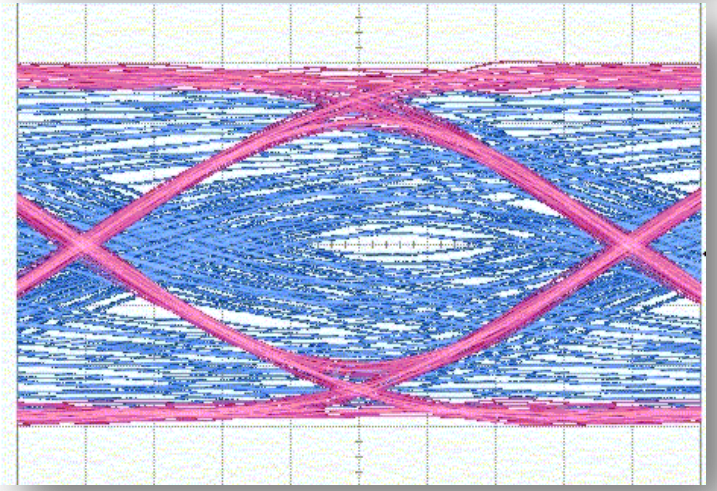


USB 3.0	4.8 Gb/s
HDMI	5 Gb/s
DVI	8 Gb/s
DP	8.6 Gb/s
PCIe	5 Gb/s
SATA	3 Gb/s
DDR3	0.8-2.133 Gb/s

- Increased Density
- High-speed everywhere
- Pressure to Reduce cost

Consequences of Serial Signaling





Less width, but…

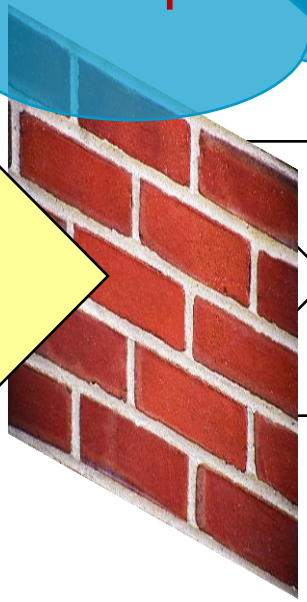
- Faster (clocks *and* edges)
  → more signal integrity issues
- Deeper → more data to manage
- Protocol → more complex debug

And…

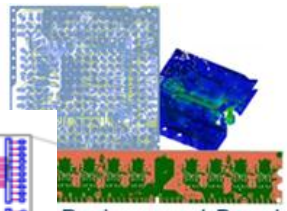
- Physical/structural layer is critical
- Multilane (width!), multilevel
- Standards evolve every 2-3 years

What's the Problem we want to Solve?

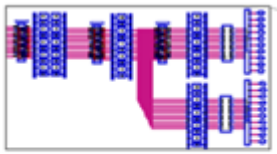
- Board/chip respin cost?
- Lost time to market?
- Can we fulfil compliance tests?



Interconnect Design → **System Design** → **Analysis Debug** → **Compliance Test**

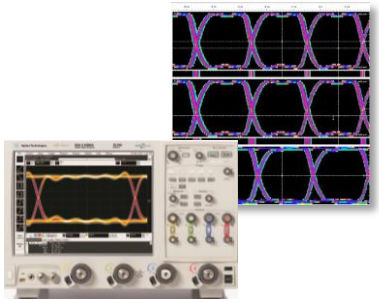


Package and Board Level Simulation



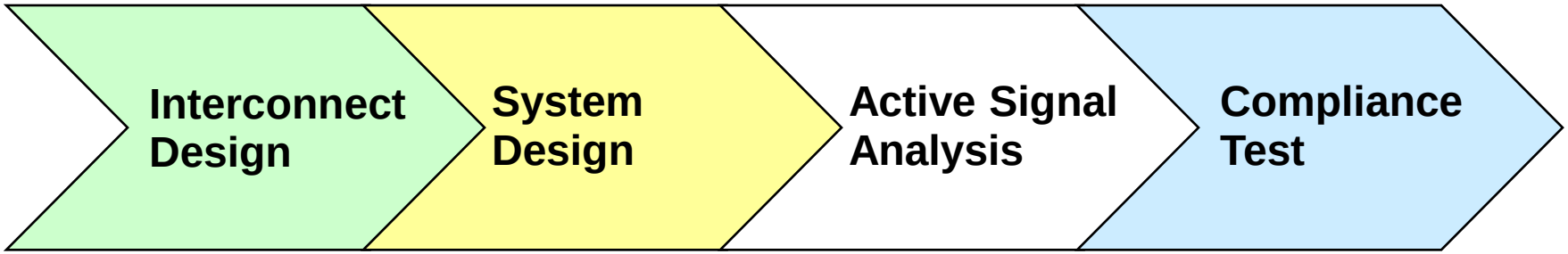
High Speed Channel Design

Protocol-based Analysis tools



10GBASE-KR
DDR2 and DDR3
PCIe
SRIO
CPRI
...

Evolving the Digital Development Process

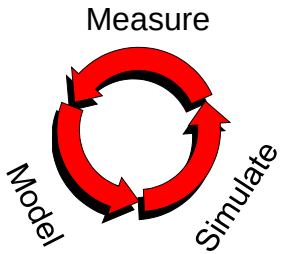


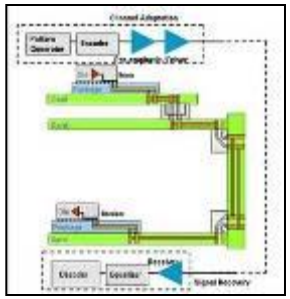
- Accurate Models
- Accurate Simulations
- Hardware & Software Correlation

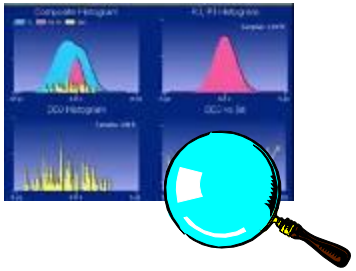
- Accurate Models & Simulations
- Accurate Design Analysis
- Hardware & Software Correlation

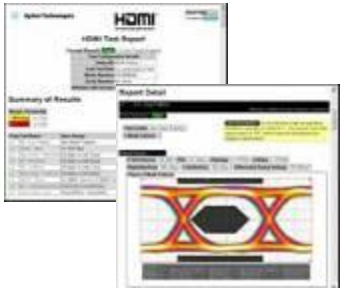
- Accurate Design Analysis
- Test & Analysis Capability
- Measurement Automation

- Increased Team Effectiveness
- Measurement Automation
- Test & Analysis Capability

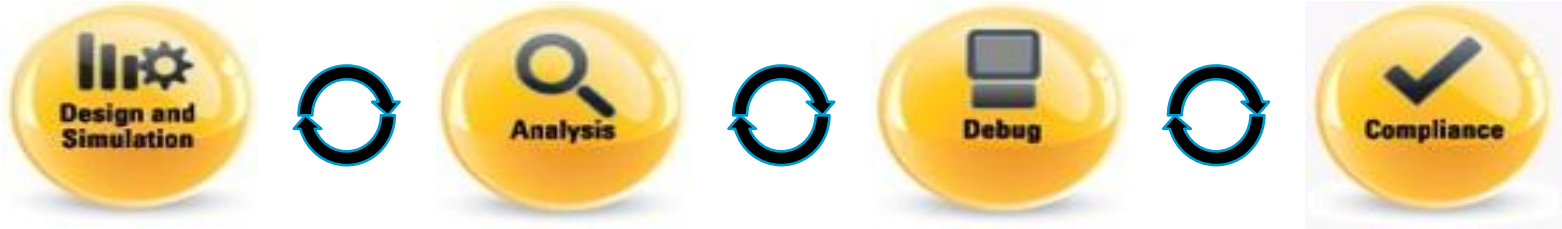








Agilent flow for High Speed Digital Design



- Channel Analysis & Optimization in Time and Freq. Domains
- Fast, Robust & Accurate Convolution Algorithms.
- Effective PCB Pre-Layout Design
- Full range of EM extraction tool
- Power Delivery Network impedance extraction
- Near field and current visualization at physical level
- Libraries for HSD PHY Compliance

- Impedance Profile Analysis TDR/TDT
- Reflections Optimization
- Time Domain Gated Filter
- Accurate Sparameters Embedding/De-Embedding
- Crosstalk's impact on EyeDiagram
- Jitter Breakdown TJ/RJ/DJ/BUJ/PJ/ISI
- Seamless integration of De-emphasis and Equalization algorithms
- Hot S11 on Live Transmitting Devices

- Fixturing De-embedding
- Reference Channel Embedding
- HighZ Probes
- Receiver emulation Equalization, CDR
- RootCause Analysis of EyeMask Collapse
- Jitter sources Analysis through Jitter FFT and Breakdown.

- Agilent member of Body standards: PCI Sig, USB Org, SATA IO, HDMI, Displayport, Thunderbolt…
- First Silicon ready TX/RX Compliance
- Accurate RX Jitter Tolerance Characterization
- Complete Protocol Validation
- Custom Compliance Test through User Defined App.

Today's Agenda

09:00	Registration
09:30	Welcome
09:45	Key Challenges in the analysis and design of high speed digital links
10:45	Break
11:00	Why Use Simulation Tools for High Speed Signal Channel Design?
12:00	Measurement Techniques of Serial Signal and Fast Rise Time Signals
13:00	Lunch & Networking
14:00	A Day in the Life of a Memory System Architect
14:45	Towards HSD Success in the Multigigabit/s Era
15:30	Conclusion