

Keysight M3602A, Graphical FPGA Design Environment

2.01.18 Version Information

Released Date:	August, 2017
Operative systems:	Microsoft Windows 7, 10 (32-bit and 64-bit OS) openSUSE 64-bit OS
Supported Modules:	M3100A, M3102A, M3201A, M3202A, M3300A, M3302A
File Name:	Windows: M3602A_2.01.18_installer.exe Linux: M3602A-2.01.18-x86_64.7z

New Features

- Improved “Firmware Loader” dialog displaying information about which module is used and the expected target module of selected firmware file. It also checks the compatibility of provided file and module and notifies about incompatibilities.
- Added support for M3300A-C24-CLF instrument.
- Added new “Integrator” library IP. See description of IP for more details.
- When a firmware generation is running, a confirmation dialog appears for closing the application.

Bug Fixes

- The M3602A needs an empty folder for generating the firmware. For this reason, now the software always creates a build folder for generating firmware and its contents is removed when generation starts. It avoids to remove user data (present files in a disk location) when user specifies a non-empty directory as build directory and its contents have to be removed.
- Support UTF-8 bit character encoding as comment text. It means, for instance, the Japanese characters can be used, saved and opened in comments.
- *PCportManager* example is installed with all required libraries and it properly runs inside “bin” folder.

2.01.12 Version Information

Released Date:	June, 2017
Operative systems:	Microsoft Windows 7, 10 (32-bit and 64-bit OS) openSUSE 64-bit OS
Supported Modules:	M3100A, M3102A, M3201A, M3202A, M3300A, M3302A
File Name:	Windows: M3602A_2.01.12_installer.exe Linux: M3602A-2.01.12-x86_64.7z

New Features

- Added support for M3302A instrument.
- Support to list of names in VHDL generic or port declaration, like:


```
generic ( a, b, c: integer := 0 );
port ( a, b, c: in std_logic_vector (3 downto 0));;
```
- Verilog parameters support has been added in order to import user blocks with configurable parameters.
- Add System Verilog files as supported files to import. However, the software is available to import the same declaration syntax as Verilog-2001 standard.
- The different user entities can be reloaded and their source files can be changed from IP library view. Then, their instances are reloaded as well.

Bug Fixes

- Licensing system integration improved in order to use native EEsof License Tools.
- Compilation crash has been fixed. Now the software checks the integrity of the project before trying to generate the solution and shows different errors if the project has blocks out of date.
- Check changes of Vivado projects as external blocks has been fixed.

• 2.01.05 Version Information

Released Date:	April, 2017
Operative systems:	Microsoft Windows XP Microsoft Windows 7, 10 (32-bit and 64-bit OS) openSUSE 64-bit OS
Supported Modules:	M3100A, M3102A, M3201A, M3202A, M3300A, M3302A
File Name:	Windows: M3602A_2.01.05_installer.exe Linux: M3602A-2.01.05-x86_64.7z

Important Note

SD1 software installation is required to be able to work with any SD1 module project.

New Features

- Database version updates. The software asks for database updates to server and if there is any available update, the program asks to user for apply it.
- M3602A User Guide added and available on “Help->M3602A Help...” menu.
- An information message with result file is showed when bitstream has been generated.
- Improved license management and validation.

Bug Fixes

- M3102A-CH4-CLF hardware project with properly version.
- White spaces in file paths support (project and user IPs as well).
- Zoom fit of scene content when project is opened at first time.

2.01.00 Version Information

First software release.

Released Date:	March, 2017
Operative systems:	Microsoft Windows XP Microsoft Windows 7, 10 (32-bit and 64-bit OS) openSUSE 64-bit OS
Supported Modules:	M3100A, M3102A, M3201A, M3202A, M3300A, M3302A
File Name:	Windows: M3602A_2.01.00_installer.exe Linux: M3602A-2.01.00-x86_64.7z

Features

- User-friendly graphical FPGA programming environment
- Streamlined design process:
 - Read-to-use block library
 - Minimizes the need for FPGA-code development
 - Include VHDL, Verilog or Xilinx® VIVADO / ISE projects
 - Include MATLAB/Simulink® code
 - Include Xilinx® CORE Generator IP cores
 - Add and remove built-in resources
- One-click compiling and programming
 - FPGA cloud compiling
 - Hot programming