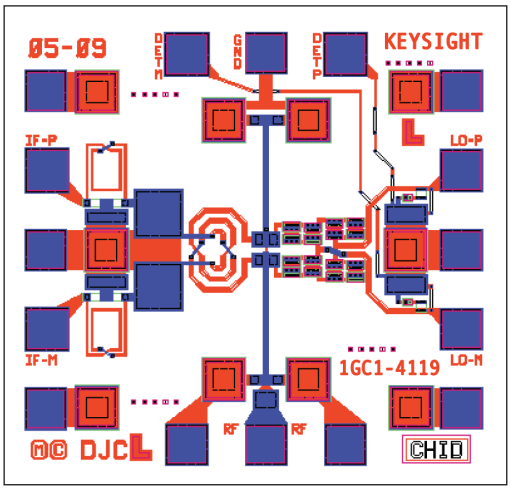
# Keysight 1GC1-4119
# 13 - 35 GHz x2
# Harmonic Mixer

## Data Sheet




### Features

- Optimized for x2 mixing
- LO range: 6.5 to 17.7 GHz
- RF range: 13 to 35 GHz
- IF range: 0 to 1 GHz
- Conversion efficiency: -11 dB typical

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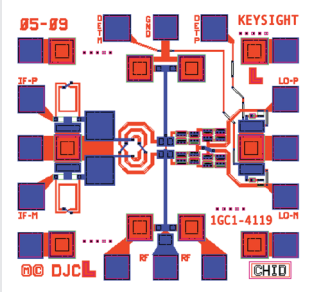
# Description

The 1GC1-4119 is a balanced mixer fabricated using Keysight's GaAs HBT process which uses anti-parallel diodes to enhance even harmonic mixing. In particular, the 1GC1-4119 has been optimized for mixing with the 2nd harmonic of a 6.5 to 17.7 GHz LO signal. Typical conversion loss is 11 dB. The LO is supplied differentially to two LO pads, LO-P and LO-M. Best conversion efficiency is obtained with approximately 13 dBm into each LO pad. The IF is extracted differentially from two IF pads, IF-P and IF-M. The RF is connected to a single pad, and applied to the diodes differentially using an on-chip balun.




- Chip Size: 930 x 880 µm (36.6 x 34.6 mils)
- Chip size tolerance: ± 10 µm (± 0.4 mils)
- Chip thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
- Pad dimensions: 80 x 80 µm ((3.15 x 3.15 mils), or larger

## Absolute maximum ratings[1]

| Symbol | Parameters/conditions | Min | Max | Units |
|---|---|---|---|---|
| $P_{in-CW}$ | Total CW input power RF + LO | | 27 | dBm |
| $V_{dc-RF}$ | RF port DC voltage | -8 | +8 | V |
| $V_{dc-LO}$ | LO-P, LO-M port DC voltage | -1.0 | +1.0 | V |
| $V_{dc-IF}$ | IF-P, IF-M port DC voltage | -1.0 | +1.0 | V |
| $V_{dc-DET}$ | DETP, DETM DC voltage | -5 | +5 | V |
| $T_j$ | Operating junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 150 | °C |
| $T_{max}$ | Max assy. temperature | | 300 | °C |
| ESD | ESD (human body model) | -300 | +300 | V |

1. $T_A$ = 25 °C except for $T_j$, $T_{stg}$, $T_{MAX}$. Operation in excess of any one of these conditions mayresult in permanent damage to the device.

## DC specifications/physical properties

($T_A$ = 25 °C, no RF or LO power applied)

| Symbol | Parameters/conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{ifp\_p1ma}$ | DC voltage at VIF-P with 1 mA at VIF-P and -1 mA at VIF-M | 1.00 | 1.32 | 1.80 | V |
| $V_{ifpm1ma}$ | DC voltage at VIF-P with -1 mA at VIF-P and 1 mA at VIF-M | -1.80 | -1.32 | -1.00 | V |
| $V_{ifmp1ma}$ | DC voltage at VIF-M with 1 mA at VIF-M and -1 mA at VIF-P | 1.00 | 1.32 | 1.80 | V |
| $V_{ifmm1ma}$ | DC voltage at VIF-M with -1 mA at VIF-M and 1 mA at VIF-P | -1.80 | -1.32 | -1.00 | V |
| $V_{ifpp5ma}$ | DC voltage at VIF-P with 5 mA at VIF-P and 5 mA at VIF-M | 1.20 | 1.46 | 2.00 | V |
| $V_{ifpm5ma}$ | DC voltage at VIF-P with -5 mA at VIF-P and 5 mA at VIF-M | -2.00 | -1.46 | -1.20 | V |
| $V_{ifmp5ma}$ | DC voltage at VIF-M with 5 mA at VIF-M and -5 mA at VIF-P | 1.20 | 1.46 | 2.00 | V |
| $V_{ifmm5ma}$ | DC voltage at VIF-M with -5 mA at VIF-M and 5 mA at VIF-P | -2.00 | -1.46 | -1.20 | V |

## RF specifications[1]

($T_A$ = 25 °C)

| Symbol | Parameters/conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $LO_{6\_5\_p14}$ | Conversion efficiency, x2 mixing mode, LO 6.5 GHz at 14 dBm | -30 | -14.5 | -5 | dB |
| $V_{Detp}$ | DC voltage at DETP for LO 6.5 GHz 16 dBm | 0.5 | 0.82 | 2.5 | V |
| $V_{Detm}$ | DC voltage at DETM for LO 6.5 GHz 16 dBm | 0.5 | 1.7 | 2.5 | V |

1. Conversion efficiency is a single-ended measurement taken at IF-P. IF frequency 50 MHz; extracted through DC probecard (loss not calibrated). RF frequency on high side of 2x LO frequency. LO is applied to LO-P and LO-M using a single 300 µm pitch Ground-Signal Picoprobe as a balun.

# Applications

The 1GC1-4119 is designed for microwave instrumentation, such as spectrum analyzers. It is used for downconversion of 13-34 GHz signals.

# Operation

Typically, around 13 dBm of LO power is applied to each LO pad. If more LO power is applied, the conversion efficiency may begin to decrease, but the third order intermodulation will improve.

The IF is extracted differentially from the IF-P and IF-M pads. Typically a ferrite balun will be used off-chip to combine these into a single IF signal.

There are detectors provided for each LO pad, DETP and DETM, which can be used for calibration or troubleshooting. Dc current at these pads should be kept to a minimum to prevent loading the LO ports (i.e., connect these pads to op-amps).

The RF port has an on-chip dcblocking capacitor; the LO and IF ports are DC coupled.

# Assembly Techniques

Epoxy die–attach using conductive epoxy or solder die–attach using a fluxless AuSu solder preform can be used for assembly. Gold thermosonic wedge bonding with 0.7 mil diameter Au wire is recommended for all bonds. Tool force should be 22 ±1 gram, stage temperature should be 150 ±2 °C; and ultrasonic power and duration should be 64 ±1 dB, and 76 ±8 msec, respectively. The bonding pad and chip backside metallization is gold. GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability. Keysight Technologies, Inc. document, *GaAs MMIC ESD, Die Attach and Bonding Guidelines - Application Note* (5991-3484EN) provides basic information on these subjects.

# RoHS Compliance

This device is RoHS Compliant. This means the component meets the requirements of the European Parliament and the Council of the European Union Restriction of Hazardous Substances Directive 2011/65/EU, commonly known as RoHS. The six regulated substances are lead, mercury, cadmium, chromium VI (hexavalent), polybrominated biphenyls (PBB) and polybrominated biphenyl ethers (PBDE). RoHS compliance implies that any residual concentration of these substances is below the RoHS Directive's maximum concentration values (MVC); being less than 1000 ppm by weight for all substances except for cadmium which is less than 100 ppm by weight.

# ESD and Handling Precautions

GaAs MMICs in either chip or SMT packages are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability. Keysight Technologies document, *GaAs MMIC ESD, Die Attach and Bonding Guidelines - Application Note* (5991-3484EN) provides basic information on these subjects.

# 1GC1-4119 Bond pad locations

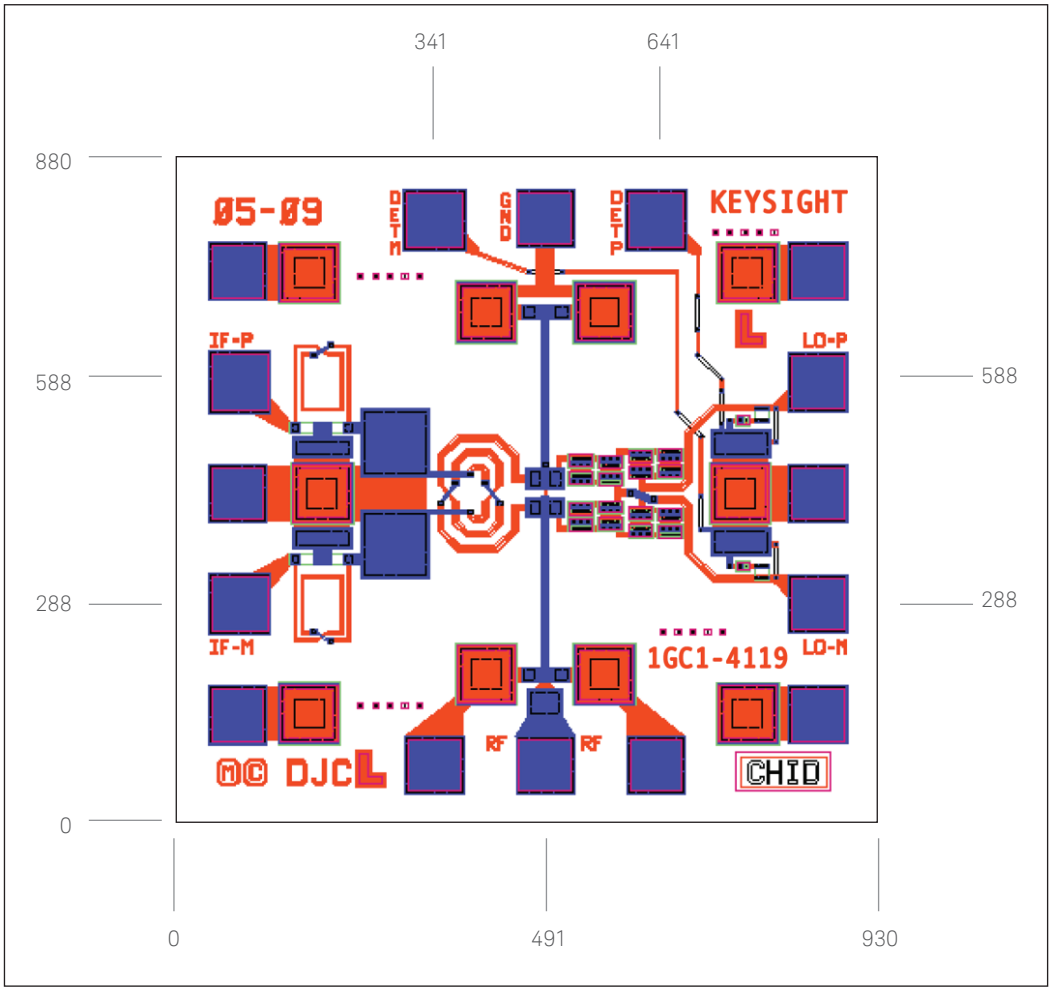
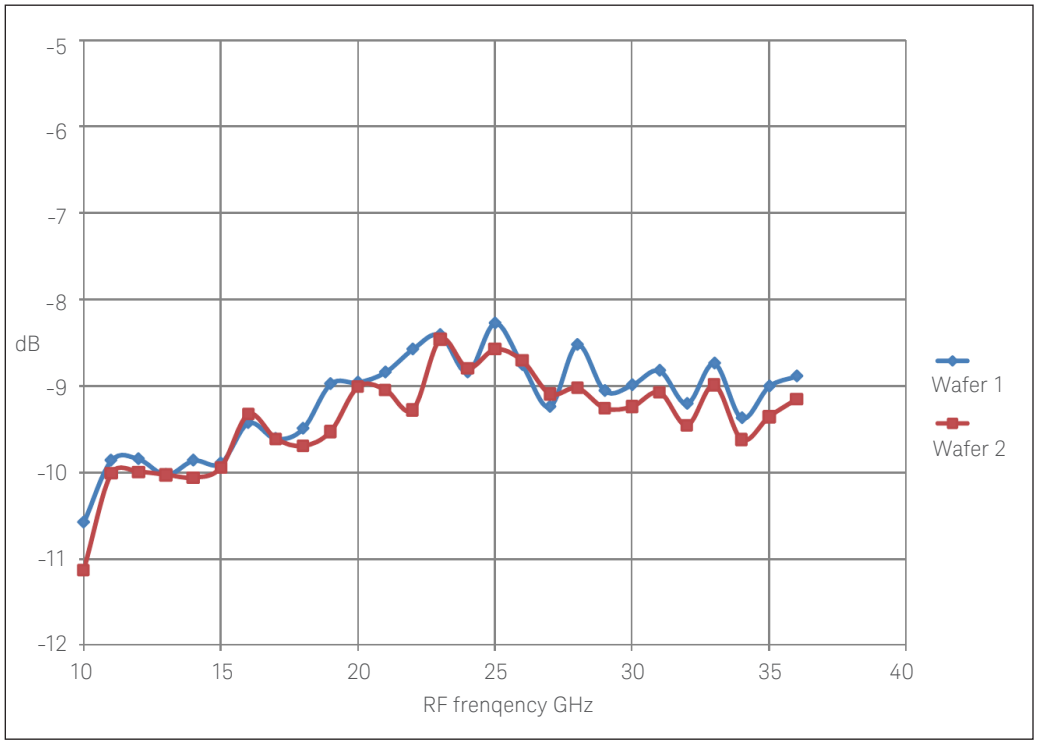



Figure 1. Bond pad locations

Notes:
All dimensions in microns.

1. Rectangular paddimensions: 80 x 80 µm
2. All other dimensions: ±5 µm (unless otherwise noted)
3. Chip thickness: 127 ±15 µm

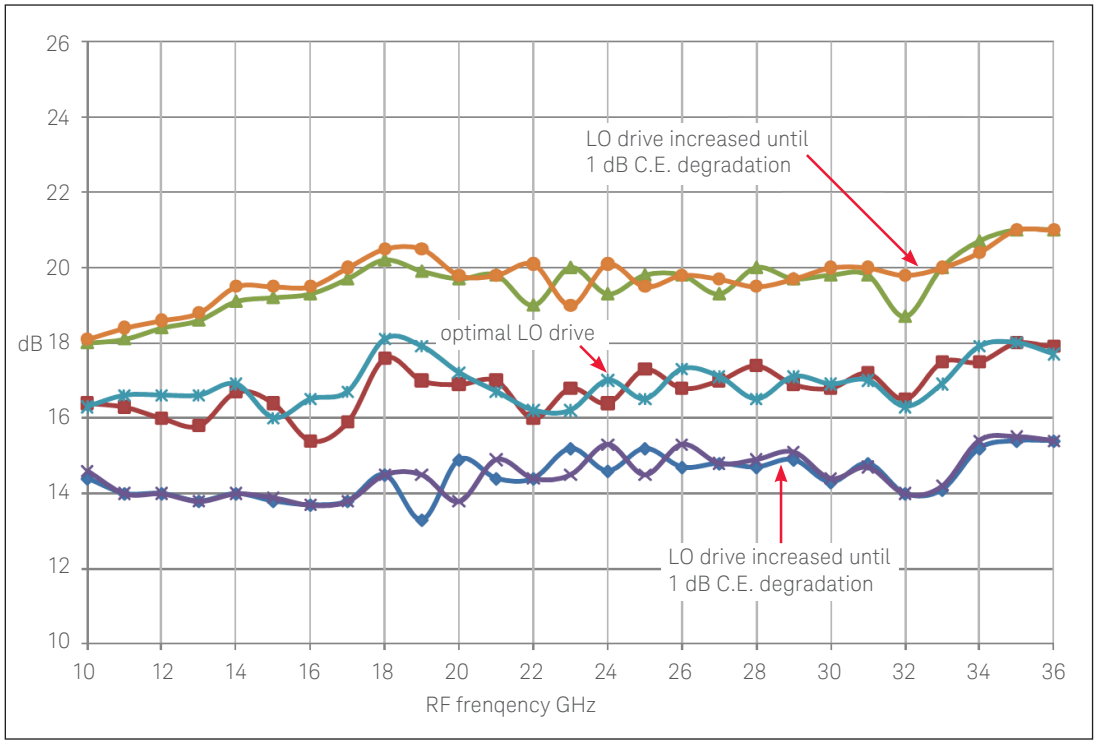
## 1GC1-4119 Conversion loss x2 mode




Notes:
All dimensions in microns.
1. 2 wafers from prototype lots
2. IF 50 MHz
3. LO optimized at each point

Figure 2. Conversion loss x 2 mode

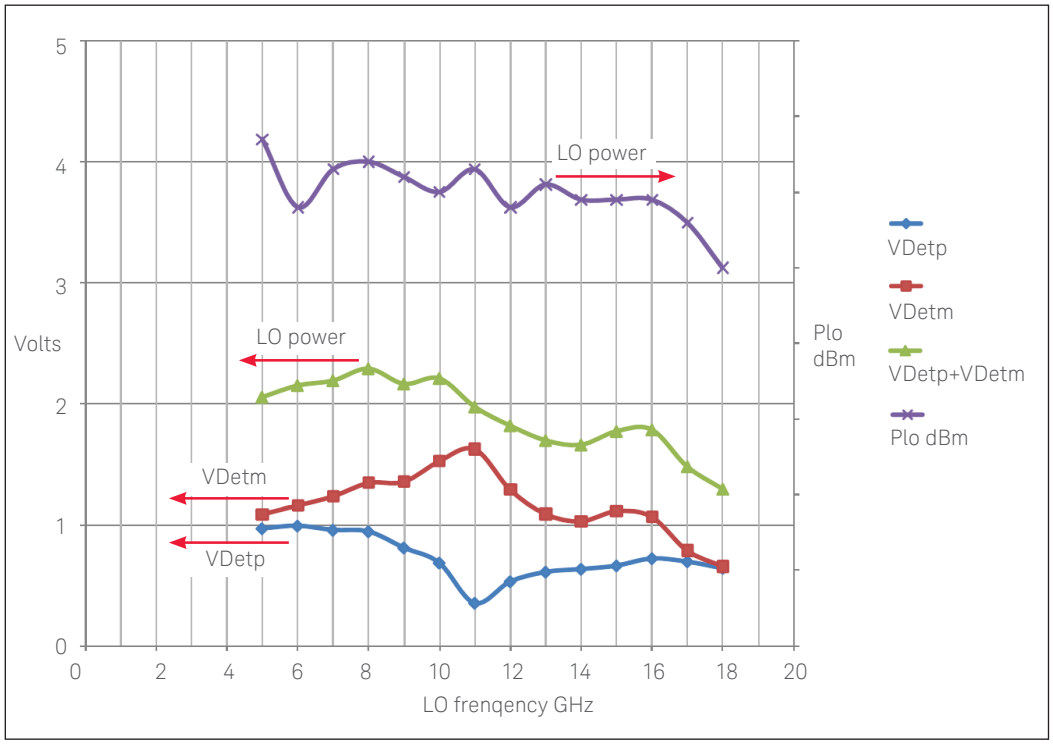
## Total LO power for optimum conversion loss and window for 1 dB increase in conversion loss




Notes:
All dimensions in microns.
1. 2 wafers from prototype lots
2. IF 50 MHz

Figure 3. LO Power for optimum conversion loss

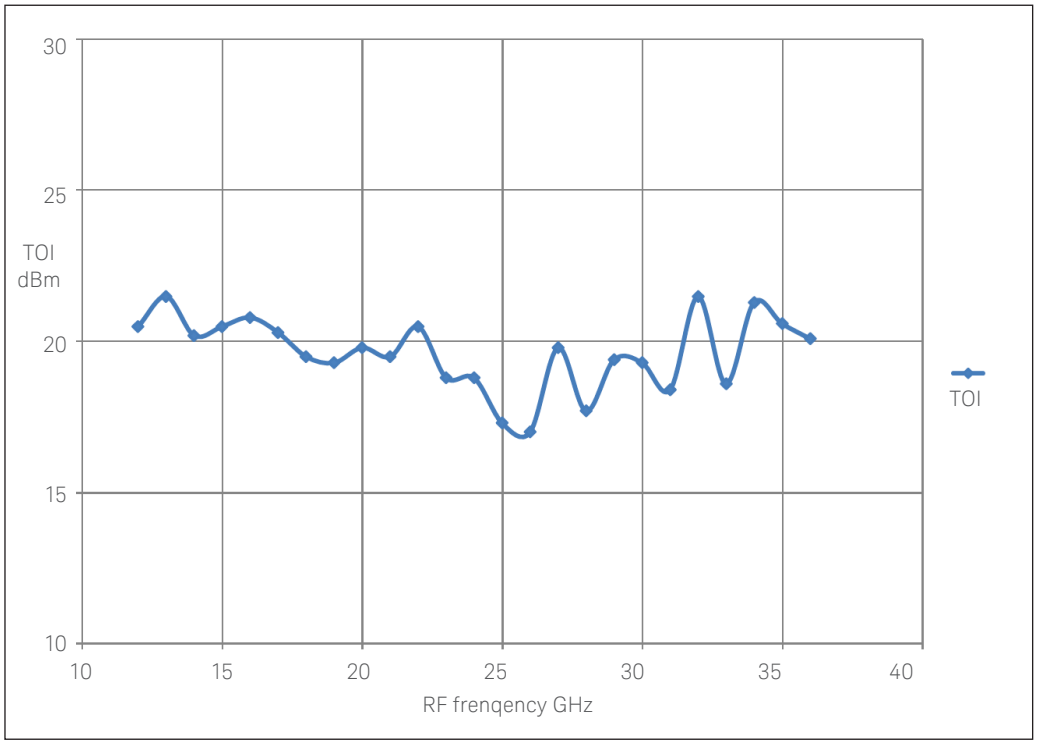
## 1GC1-4119 Detector voltages




Notes:
300 µm pitch G-S probe used to inject LO; loss not incl

Figure 4. Detector voltages

## 1GC1-4119 TOI




Notes:
1. LO drive set 1 dB above optimum C.E.
2. IF 50 MHz

Figure 5. 1GC1-4119 TOI

## 1GC1-4119 Schematic

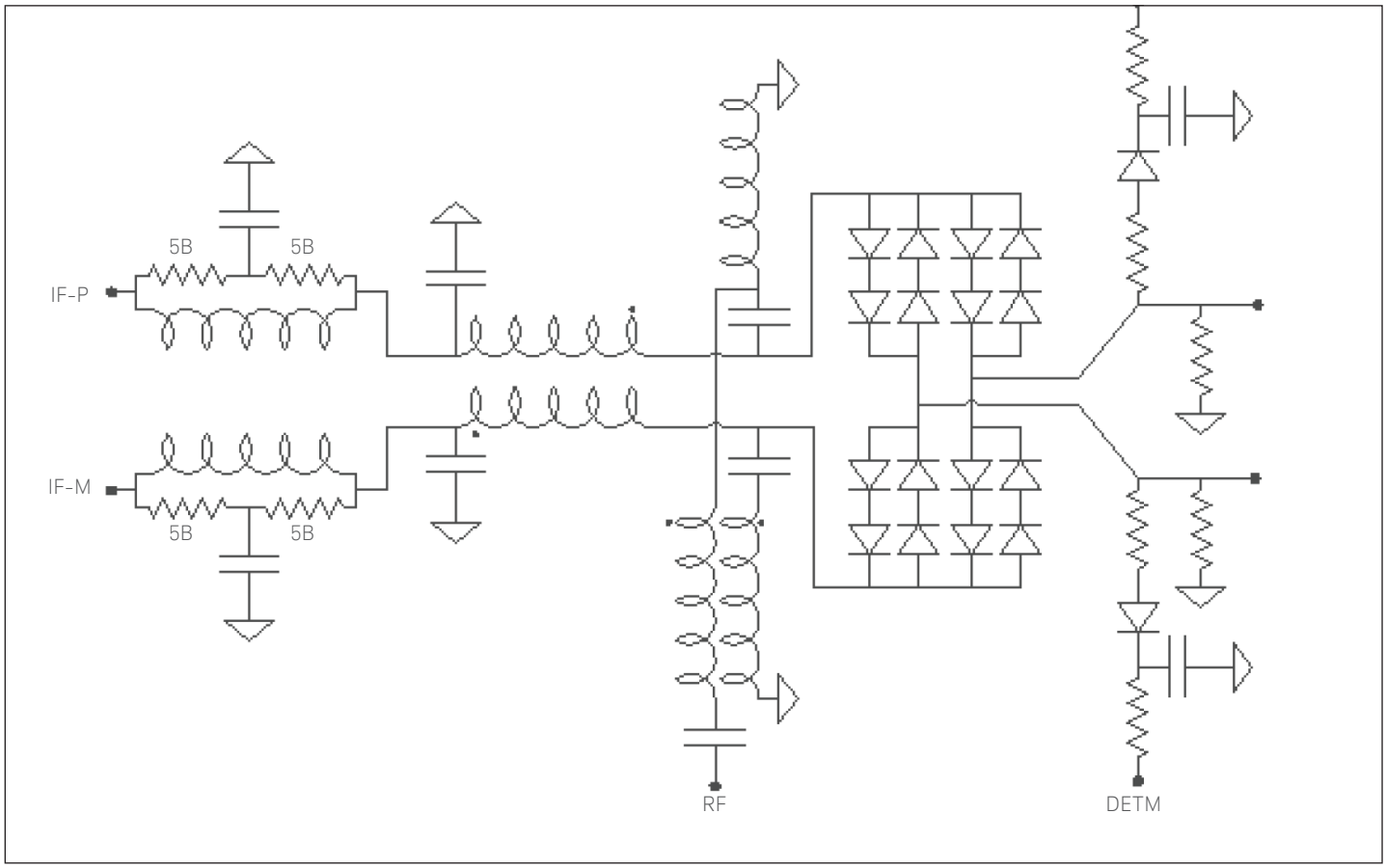



Figure 6. 1GC1-4119 Schematic

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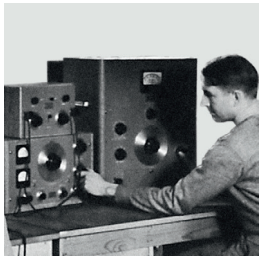

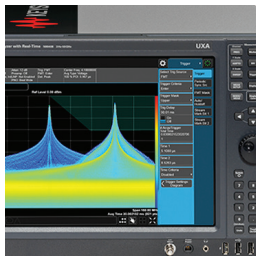

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The product described in this data sheet is RoHS Compliant. See RoHS Compliance section for more details.

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