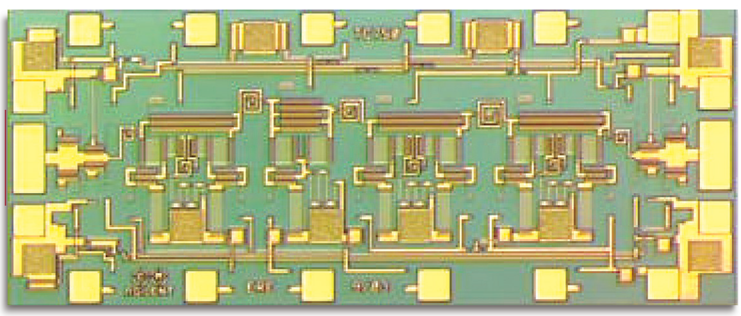
Keysight 1GG7-4103
DC-12 GHz 35 dB/5 dB Electronic Step Attenuator

Data Sheet



Features

- Frequency range: DC to 12 GHz
- Attenuation values: 0 to 35 in 5 dB Steps
- Insertion loss: 6.1 dB @ 10 GHz
- Return loss: 20 dB @ 10 GHz
- Switching speed: < 1 µs (10% to 90% T_R)
- Distortion
  SHI: +81 dBm
  THI: +52 dBm
  TOI: +55 dBm
- P_{-1dB}: 29 dBm @ 10 GHz

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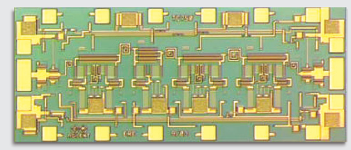
Description

The 1GG7-4103 is a 35 dB by 5 dB step GaAs MMIC step attenuator designed for good input match and low distortion from DC to 12 GHz. It is intended for use as a high-performance solid–state step–attenuator for RF instrumentation applications.

Each attenuator cell incorporates a “bridged–T” topology with series and shunt MESFET switching elements. Bias to the gate of the FET switches is through a resistor and a diode which improves distortion at low frequencies. Shunt resistors at the input and output ports can be switched on or off to optimize input match. Ground connection is through backside vias. The 1GG7-4103 is fabricated with Keysight Technologies, Inc. GaAs FET MMIC process.



- Chip size:
  1790 x 760 (70.5 x 29.9 mils)
- Chip size tolerance:
  ±10 µm (±0.4 mils)
- Chip thickness:
  127 ±15 µm (5.0 ±0.6 mils)
- Small pad dimensions:
  80 x 80 µm (3.1 x 3.1 mils)
- Large pad dimensions:
  80 x 170 µm (3.1 x 6.7 mils)

Absolute maximum ratings[1]

Symbol	Parameters/conditions	Min.	Max.	Units
$VR_{R1\text{-}R4,\ C10A\&B,\ C20A\&B2}$	Control line voltages	-10	+10	Volts
$V_{(in/out)}$	Input/output voltage (total DC+RF)	-5	+5	Volts
$I_{(in/out)}$	Input/output current (DC)	-100	+100	mA
T_{bs}	Maximum backside temperature		+70	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature		+300	°C

1. Operation in excess of any one of these may result in permanent damage to this device.

DC specifications/physical properties

(T_A = 25 °C)

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
$V_{R1\text{-}R4,\ C5A\&B,\ C10A\&B,\ C20A\&B(+)}$	Positive control line voltage	7	10	10	Volts
$V_{R1\text{-}R4,\ C5A\&B,\ C10A\&B,\ C20A\&B(-)}$	Negative control line voltage	-10	-10	-7	Volts
$I_{L(+)}$	Positive control line leakage current ($V_{R1\text{-}R4,C5A\&B,C10A\&B,C20A\&B}$ = +10 V)			50	µA
$I_{L(-)}$	Negative control line leakage current ($V_{R1\text{-}R4,C5A\&B,C10A\&B,C20A\&B}$ = –10 V)			50	µA
R1	Input and output R1 shunt trim resistor		371		Ohms
R2	Input and output R2 shunt trim resistor		742		Ohms
R3	Input and output R3 shunt trim resistor		1484		Ohms
R4	Input and output R4 shunt trim resistor		2967		Ohms

Typical attenuation temperature coefficients

Symbol	Parameters/conditions			Units
	Frequency	**50 MHz**	**1 GHz**	
α_T	@ Minimum insertion loss state	0.0026	0.0018	dBc/ °C
	@ 5 dB state	0.0002	-0.0008	
	@ 10 dB state	-0.0015	-0.0026	
	@ 15 dB state	-0.0034	-0.0047	
	@ 20 dB state	-0.0043	-0.0060	
	@ 25 dB state	-0.0064	-0.0078	
	@ 30 dB state	-0.0072	-0.0095	
	@ 35 dB state	-0.0096	-0.0122	

RF specifications

(T_A = 25 °C, Z_0 = 50 Ω, $V_{Control\ lines}$ = ±10 volts, trim resistors as specified in logic table)

		1 GHz			10 GHz			
Symbol	**Parameters/conditions**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Rin_0	Rin @ 0 dB state	43	49	54				Ohms
Rin_5	Rin @ 5 dB state	42	49	56				Ohms
Rin_10	Rin @ 10 dB state	41	49	57				Ohms
Rin_20	Rin @ 20 dB state	41	49	57				Ohms
Rin_35	Rin @ 35 dB state	41	49	58				dB
S11_0	S11 @ 0 dB state			-25			-17	dB
S11_5	S11 @ 5 dB state			-24			-17	dB
S11_10	S11 & 10 dB state			-22			-19	dB
S11_20	S11 @ 20 dB state			-21			-16	dB
S11_35	S11 @ 35 dB state			-22			-17	dB
S22_0	S22 @ 0 dB state			-25			-17	dB
S22_5	S22 @ 5 dB state			-24			-16	dB
S22_10	S22 @ 10 dB state			-22			-19	dB
S22_20	S22 @ 20 dB state			-21			-16	dB
S22_35	S22 @ 35 dB state			-22			-16	dB
S21_0	S21 @ 0 dB state	-5.1		-3.3	-7.5		-4.7	dB
S21_5	S21 @ 5 dB state	-10.3		-8.9	-12.7		-10.3	dB
S21_10	S21 @ 10 dB state	-15.6		-14.2	-17.4		-15	dB
S21_20	S21 @ 20 dB state	-26.2		-24	-27.6		-24.8	dB
S21_35	S21 @ 35 dB state	-43.1		-37.7	-44.1		-38.5	dB
S12_0	S12 @ 0 dB state	-5.1		-3.3	-7.5		-4.7	dB
S12_5	S12 @ 5 dB state	-10.3		-8.9	-12.7		-10.3	dB
S12_10	S12 @ 10 dB state	-15.6		-14.2	-17.4		-15	dB
S12_20	S12 @ 20 dB state	-26.2		-24	-27.6		-24.8	dB
S12_35	S12 @ 35 dB state	-43.1		-37.7	-44.1		-38.5	dB
SHI	2nd Harmonic intercept point (Referred to P_{in})					81		dBm
THI	3rd Harmonic intercept point (Referred to P_{in})					52		dBm
TOI	Two-tone 3rd order intercept point (Referred to P_{in})	55 dBm typ. @ 3 GHz						dBm
P_{1dB}	Input power @ 1 dB increase or decrease in insertion loss	29 dBm typ. @ 3 GHz						dBm

Applications

The 1GG7-4103 is designed for use in instrumentation, communications, radar, ECM, EW, and many other systems requiring fast switching speed, low distortion to input signals, and high cycle lifetimes. It can be used for pulse modulation, port isolation, replacement of mechanical relays, and in any application requiring the advantages of solid-state performance.

This device does not include any on–chip driver circuitry. An external driver circuit is required to convert TTL or ECL logic signals to the ±10 volt switching levels required by this device.

Figure 3 shows the device assembly diagram for operation through 12 GHz. Dual RF input and output bonds are recommended for assemblies where the device to thin film circuit gap exceeds 10 mils.

Assembly Techniques

This device is compatible with Au–Sn eutectic or conductive epoxy processes. Gold thermosonic ball or wedge bonding is recommended for all wire bonds. The bond pads are designed to be large enough to facilitate auto-bonding. The top and bottom metallization is gold.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Keysight document, *GaAs MMIC ESD, Die Attach and Bonding Guidelines - Application Note* (5991-3484EN) provides basic information on these subjects.

Logic table

"1" corresponds to "+10 V control line voltage"
"0" corresponds to "-10 V control line voltage"
Typical trim resistors controls for best match

Attenuation setting	R1	R2	R3	R4	C5A	C5B	C10A	C10B	C20A	C20B
Min. insertion loss	0	1	0	0	1	0	1	0	1	0
5 dB state	0	1	1	0	0	1	1	0	1	0
10 dB state	0	1	1	1	1	0	0	1	1	0
15 dB state	0	1	1	1	0	1	0	1	1	0
20 dB state	0	1	1	1	1	0	1	0	0	1
25 dB state	0	1	1	1	0	1	1	0	0	1
30 dB state	0	1	1	1	1	0	0	1	0	1
35 dB state	0	1	1	1	0	1	0	1	0	1

Simplified schematic

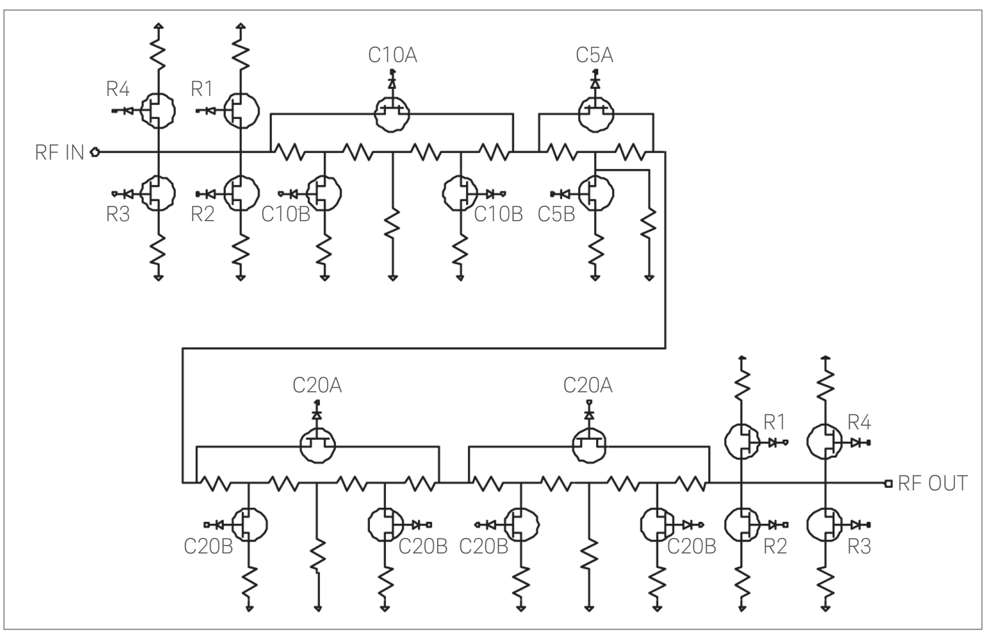


Figure 1. 1GG7-4103 simplified schematic

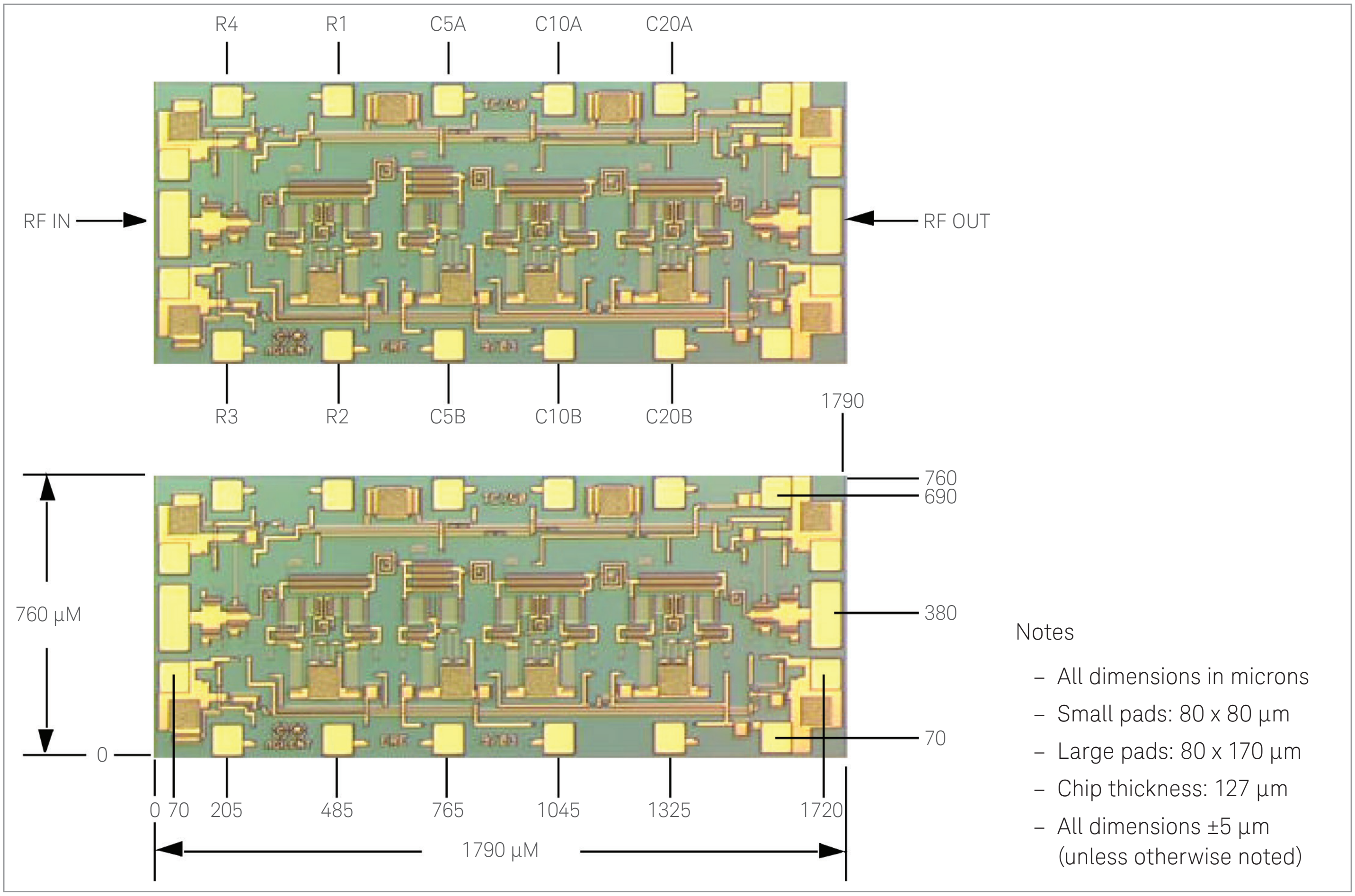


Figure 2. 1GG7-4103 bond pad locations

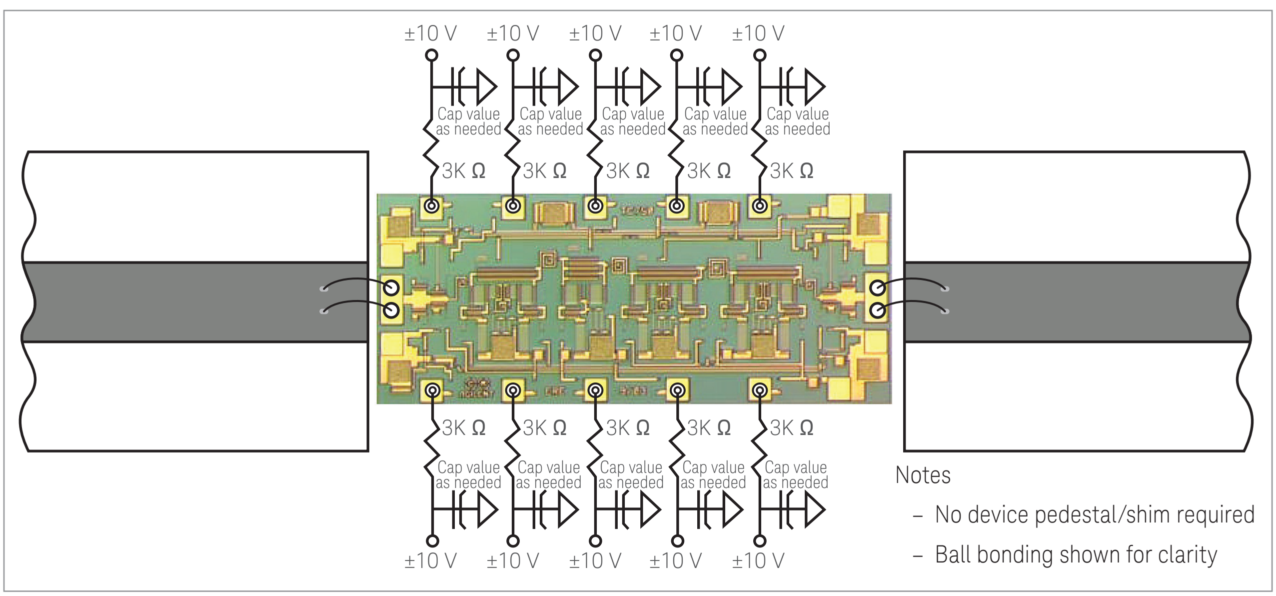


Figure 3. 1GG7-4103 assembly diagram

Supplemental Data

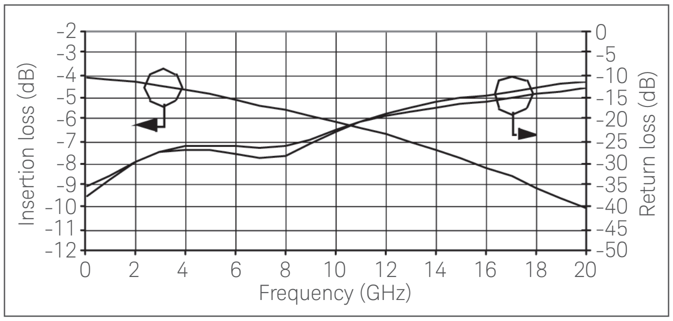


Figure 4. Minimum insertion loss and return loss vs. frequency

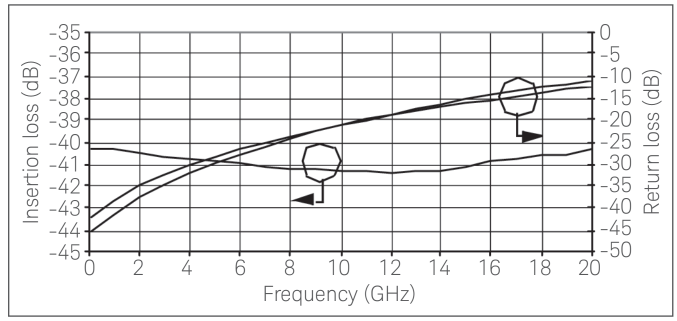


Figure 5. Insertion loss @ 35 dB state and return loss vs. frequency

Typical S-parameters: 0 dB state (minimum insertion loss state)[1]

Frequency (GHz)	S_{11}			S_{12} and S_{21}			S_{22}		
	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
0.1	-35.437	0.017	172.725	-4.127	0.622	-1.822	-37.423	0.013	170.929
1	-33.030	0.022	131.505	-4.213	0.616	-16.371	-34.012	0.020	124.942
2	-29.619	0.033	102.803	-4.355	0.606	-32.158	-29.761	0.033	98.255
3	-27.666	0.041	84.142	-4.528	0.594	-47.652	-27.408	0.043	82.295
4	-26.839	0.046	71.785	-4.713	0.581	-62.880	-26.309	0.048	71.330
5	-27.047	0.044	64.844	-4.911	0.568	-77.968	-26.014	0.050	65.235
6	-28.024	0.040	65.184	-5.125	0.554	-92.977	-26.378	0.048	64.528
7	-29.019	0.035	77.258	-5.355	0.540	-107.875	-26.807	0.046	71.327
8	-28.315	0.038	97.193	-5.585	0.526	-122.791	-26.453	0.048	83.544
9	-25.638	0.052	111.351	-5.836	0.511	-137.654	-24.787	0.058	94.612
10	-22.892	0.072	115.726	-6.104	0.495	-152.595	-22.783	0.073	99.870
11	-20.580	0.094	114.666	-6.399	0.479	-167.450	-20.956	0.090	100.976
12	-18.771	0.115	111.784	-6.714	0.462	177.676	-19.466	0.106	99.867
13	-17.382	0.135	107.804	-7.045	0.444	162.793	-18.284	0.122	97.640
14	-16.303	0.153	104.604	-7.417	0.426	147.930	-17.384	0.135	95.788
15	-15.376	0.170	101.392	-7.797	0.408	133.138	-16.596	0.148	94.365
16	-14.580	0.187	98.760	-8.202	0.389	118.263	-15.919	0.160	93.605
17	-13.781	0.205	96.499	-8.641	0.370	103.456	-15.184	0.174	92.888
18	-13.024	0.223	93.957	-9.101	0.351	88.685	-14.448	0.189	92.186
19	-12,324	0.242	91.274	-9.589	0.332	73.960	-13.710	0.206	91.379
20	-11.714	0.260	88.368	-10.100	0.313	59.096	-12.982	0.224	89.793

1. Wafer probed data with simulated double 20–mil long bond wires added to RF_IN and RF_Out pads. Control line voltages are listed in Logic Table .T_A = +25 °C.

Typical S–parameters: 35 dB state[1]

Frequency (GHz)	S_{11}			S_{12} and S_{21}			S_{22}		
	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
0.1	-41.949	0.008	172.108	-40.342	0.0096	-1.872	-45.105	0.006	175.802
1	-38.542	0.012	146.704	-40.359	0.0096	-10.042	-41.819	0.008	147.173
2	-34.978	0.018	126.005	-40.459	0.0095	-18.626	-37.724	0.013	128.427
3	-32.437	0.024	116.417	-40.649	0.0093	-27.253	-34.737	0.018	121.919
4	-30.184	0.031	111.767	-40.740	0.0092	-35.256	-32.278	0.024	120.252
5	-28.307	0.038	110.078	-40.808	0.0091	-43.447	-29.943	0.032	119.920
6	-26.576	0.047	109.061	-40.958	0.0090	-51.268	-27.897	0.040	120.358
7	-25.063	0.056	108.549	-41.133	0.0088	-58.773	-26.060	0.050	120.246
8	-23.721	0.065	107.852	-41.196	0.0087	-66.775	-24.376	0.060	120.153
9	-22.437	0.076	107.411	-41.193	0.0087	-73.915	-22.770	0.073	119.675
10	-21.263	0.086	106.806	-41.283	0.0086	-82.209	-21.316	0.086	118.647
11	-20.161	0.098	106.276	-41.337	0.0086	-89.057	-19.998	0.100	177.786
12	-19.37	0.110	105.754	-41.400	0.0085	-96.079	-18.777	0.115	116.643
13	-18.160	0.124	104.726	-41.337	0.0086	-103.506	-17.584	0.132	115.117
14	-17.255	0.137	104.095	-41.300	0.0086	-110.003	-16.491	0.150	113.457
15	-16.341	0.152	103.010	-41.106	0.0088	-118.219	-15.441	0.169	111.601
16	-15.502	0.168	102.000	-40.808	0.0091	-125.348	-14.484	0.189	109.552
17	-14.650	0.185	100.737	-40.743	0.0092	-134.248	-13.573	0.210	107.091
18	-13.829	0.203	98.995	-40.583	0.0094	-143.793	-12.720	0.231	104.380
19	-13.072	0.222	97.105	-40.553	0.0094	-151.522	-11.933	0.253	101.981
20	-12.407	0.240	95.203	-40.320	0.0096	-160.693	-11.207	0.275	99.106

1. Wafer probed data with simulated double 20–mil long bond wires added to RF_IN and RF_Out pads. Control line voltages are listed in logic table. T_A = +25 °C.

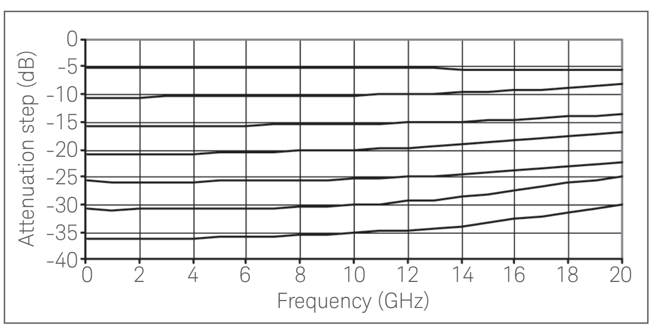


Figure 6. Attenuation step values vs. frequency

Attenuation step values vs frequency[1]

T_A = +25 °C

Frequency (GHz)	5 dB state (dB)	10 dB state (dB)	15 dB state (dB)	20 dB state (dB)	25 dB state (dB)	30 dB state (dB)	35 dB state (dB)
0.1	-5.39	-10.64	-15.69	-20.78	-25.81	-30.91	-36.22
1	-5.43	-10.66	-15.76	-20.86	-25.94	-31.03	-36.15
2	-5.43	-10.63	-15.75	-20.84	-25.96	-30.98	-36.10
3	-5.42	-10.59	-15.71	-20.80	-25.90	-30.98	-36.12
4	-5.41	-10.54	-15.68	-20.74	-25.88	-30.92	-36.03
5	-5.41	-10.50	-15.64	-20.66	-25.82	-30.83	-35.90
6	-5.41	-10.45	-15.61	-20.60	-25.76	-30.73	-35.83
7	-5.41	-10.40	-15.57	-20.54	-25.71	-30.61	-35.78
8	-5.43	-10.36	-15.52	-20.43	-25.56	-30.50	-35.61
9	-5.43	-10.30	-15.47	-20.30	-25.47	-30.31	-35.36
10	-5.45	-10.24	-15.43	-20.18	-25.31	-30.12	-35.18
11	-5.46	-10.16	-15.35	-19.99	-25.19	-29.82	-34.94
12	-5.46	-10.06	-15.24	-19.74	-25.00	-29.51	-34.69
13	-5.49	-9.92	-15.11	-19.50	-24.73	-29.12	-34.29
14	-5.50	-9.79	-14.98	-19.24	-24.41	-28.66	-33.88
15	-5.51	-9.61	-14.84	-18.90	-24.05	-28.15	-33.31
16	-5.51	-9.41	-14.59	-18.52	-23.74	-27.60	-32.61
17	-5.55	-9.17	-14.39	-18.08	-23.35	-26.86	-32.10
18	-5.56	-8.91	-14.09	-17.64	-22.96	-26.14	-31.48
19	-5.58	-8.62	-13.86	-17.24	-22.73	-25.59	-30.96
20	-5.60	-8.28	-13.51	-16.78	-22.29	-24.75	-30.22

1. Wafer probed data with simulated double 20-mil long bond wires added to RF_IN and RF_Out pads. Control line voltages are listed in logic table. T_A = +25 °C.

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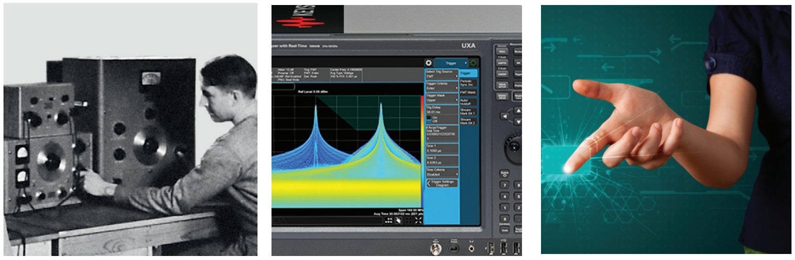

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Published in USA, September 27, 2016
5992-1818EN
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