

# Keysight 1GC1-4293

DC-26.5 (50) GHz, GaAs HBT MMIC,  
Packaged Limiter

Data Sheet



## Features

- Broadband frequency coverage, specified to 26.5 GHz, usable to 50 GHz
- Two independent limiters for single-ended or differential signals.
- Ultra-flat group delay for high pulse fidelity.
- RoHS compliant SMT 2 mm x 2 mm QFN surface mount package

## Description

The 1GC1-4293 is a 26.5 GHz, packaged integrated diode limiter (usable to 50 GHz) that can be used to protect sensitive RF circuits and subsystems from excess RF power, DC transients, and ESD. The 1GC1-4293 can be used as an unbiased 10 or 18 dBm passive limiter; it also provides adjustable limiting and peak power detection capabilities up to 20 dBm. In addition to millimeter-wave analog applications, the ultra-flat group-delay, available with this MMIC, makes it an ideal input or output protection solution in time-domain pulse applications. The 1GC1-4259 is available in a 2 mm x 2 mm Quad Flat - No Leads (QFN) SMT package to preserve BW performance and save space on densely populated PC Board designs.

### Absolute maximum ratings<sup>1, 2</sup>

| Symbol          | Parameters/conditions  | Min | Max  | Units |
|-----------------|--|-----|------|-------|
| $V_{BIAS}$      | Voltage at anode ( $V_A$ )                                     | -5  |      | V     |
| $V_{BIAS}$      | Voltage at cathode ( $V_C$ )                                   |     | +5   | V     |
| $I_{BIAS}$      | Continuous forward current into $V_A$ , $V_C$                  |     | 36   | mA    |
| $V_{rev}$       | Reverse bias voltage on each diode                             |     | 8    | V     |
| $I_{fwd}$       | Forward bias current on each diode                             |     | 36   | mA    |
| $V_{in}$        | Voltage at RFin, RFout   | -5  | +5   | V     |
| $I_{IN}$        | Current at RFin, RFout   | -80 | 80   | mA    |
| $P_{in}(CW)$    | CW RF input power A & C grounded                               |     | +17  | dBm   |
| $P_{in}(Max)^3$ | Max instantaneous input power (burn-out)                       |     | 3    | W     |
| $T_{bs}$        | Package backside temperature                                   | -40 | +85  | °C    |
| $T_{stg}$       | Storage temperature  | -65 | +150 | °C    |
| $T_{assy}^4$    | Maximum solder reflow temp.<br>(max. 3 cycles @ 30 sec./cycle) |     | +260 | °C    |

- Parameters specified for continuous operation at  $T_{bs} \leq 85^\circ\text{C}$ .
- Operation in excess of any one of these conditions may result in permanent damage to this component.
- Maximum damage limit
- Refer to JEDEC J-STD-020D for detailed reflow profile, 3 reflows max.



- Package type: Quad flat - no leads (SMT QFN)
- Package dimensions: 2.0 x 2.0 mm (0.079 x 0.079 in)
- Package thickness: 0.85 ±0.10 mm (0.035 ±0.0039 in)
- Lead pitch: 0.40 mm (0.016 in)
- Lead width: 0.20 mm (0.008 in)

## DC specifications/physical properties

( $T_A = 25\text{ }^{\circ}\text{C}$  unless otherwise listed)

| Symbol                       | Parameters/conditions  | Min | Typ  | Max | Units         |
|------------------------------|--|-----|------|-----|---------------|
| $V_{fwd\_A}$<br>$V_{fwd\_C}$ | Limiting diode forward voltage @ 0.1 mA                                | 0.5 | 0.64 | 0.8 | V             |
| $V_{fwd\_D}$                 | 2-diode bias stack forward voltage @ 0.1 mA                            | 0.8 | 1.15 | 1.5 | V             |
| $R_{S\_A}$<br>$R_{S\_C}$     | Limiting diode series resistance @ 15 mA<br>(Including 2 ohm resistor) | 5   | 12   | 20  | $\Omega$      |
| $I_A, I_C$                   | Limiting diode reverse leakage current @ -1 V                          |     | 0.1  | 1.2 | $\mu\text{A}$ |
| $R_{S\_Series}$              | Through series resistance  |     | 1.2  | 5.5 | $\Omega$      |

## RF specifications

( $T_A = 25\text{ }^{\circ}\text{C}$  unless otherwise listed)

| Symbol           | Parameters/conditions  | Min | Typ              | Max | Units |
|------------------|--|-----|------------------|-----|-------|
| $S_{11}, S_{22}$ | Reflection parameters @ 26.5 GHz   |     | -15              |     | dB    |
| $S_{21}, S_{12}$ | Through loss @ 26.5 GHz  |     | -1.0             |     | dB    |
| $\Delta\tau_d$   | Group delay flatness @ DC - 26.5 GHz   |     | $\pm 1.0$        |     | pSec  |
| $P_{-1dB}$       | 1 dB gain compression (A & C grounded)   |     | 10               |     | dBm   |
|                  | 1 dB gain compression (A & C Biased)   |     | Voltage variable |     | dBm   |
| SHI              | Second harmonic intercept<br>( $f_o = 5\text{ GHz}$ , A & C grounded)                    |     | 70               |     | dBm   |
| THI              | Third harmonic intercept<br>( $f_o = 5\text{ GHz}$ , A & C grounded)                     |     | 32               |     | dBm   |
| TOI              | Third order intercept<br>( $f_1 = 5\text{ GHz}$ , $f_2 = 5\text{ GHz}$ , A & C grounded) |     | 32               |     | dBm   |

## ESD specifications<sup>1</sup>

( $T_A = 25\text{ }^{\circ}\text{C}$  unless otherwise listed)

| Symbol | Parameters/conditions          | Min | Typ  | Max | Units |
|--------|--------------------------------|-----|------|-----|-------|
| ESD    | ESD no damage (A & C grounded) |     | 2400 |     | V     |

1. Using human body model as ESD generator. Circuit equivalent is 100 pF, 1500  $\Omega$

## Applications

The 1GC1-4293 is designed for use in high frequency communication systems, microwave instrumentation, and EW radar systems as a protection circuit for ESD, DC transients, forward or reverse power protection (F/RPP), or as an RF limiter with optional power detection.

## Device Architecture

1GC1-4293 MMIC limiter can be used as a direct-coupled, differential I/O compatible limiter. Anti-parallel shunt diodes are employed to clip the RF input signal once the input voltage swing is large enough to cause the diodes to conduct.



## Moisture Compatibility

Injection mold components like the 1GC1-4293 in QFN are moisture-sensitive. The product is tested to the Moisture and Reflow Sensitivity Level 3 as per IPC/Jedec J-STD-020 and must be mounted within 168 hours of opening the shipping container. Store and handle parts for reflow and for rework per IPC/Jedec J-STD-033B. An example of the moisture sensitivity label is shown in Figure 2.

## Tape and Reel

The 1GC1-4293 is available in tape and reel format to facilitate automatic pick and place manufacturing. See Figure 3.

## RoHS Compliance

The 1GC1-4293 limiter is RoHS compliant, meeting the requirements of the EU *Restriction of Hazardous Substances* Directive 2011/65/EU, commonly known as *RoHS*. Six substances are regulated: lead, mercury, cadmium, chromium VI (hexavalent chromium), polybrominated biphenyls (PBB), and polybrominated biphenyl ethers (PBDE). RoHS compliance requires that any residual concentration of these substances is below the Directive’s maximum concentration values (MCV): cadmium 100 ppm by weight and all others 1000 ppm by weight.

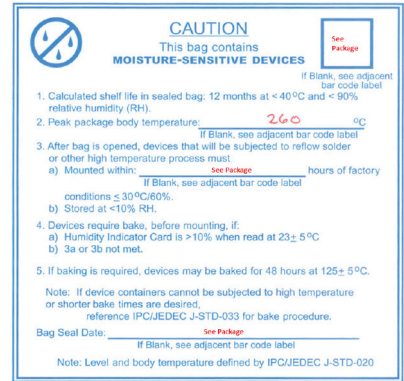


Figure 2. Moisture sensitivity label

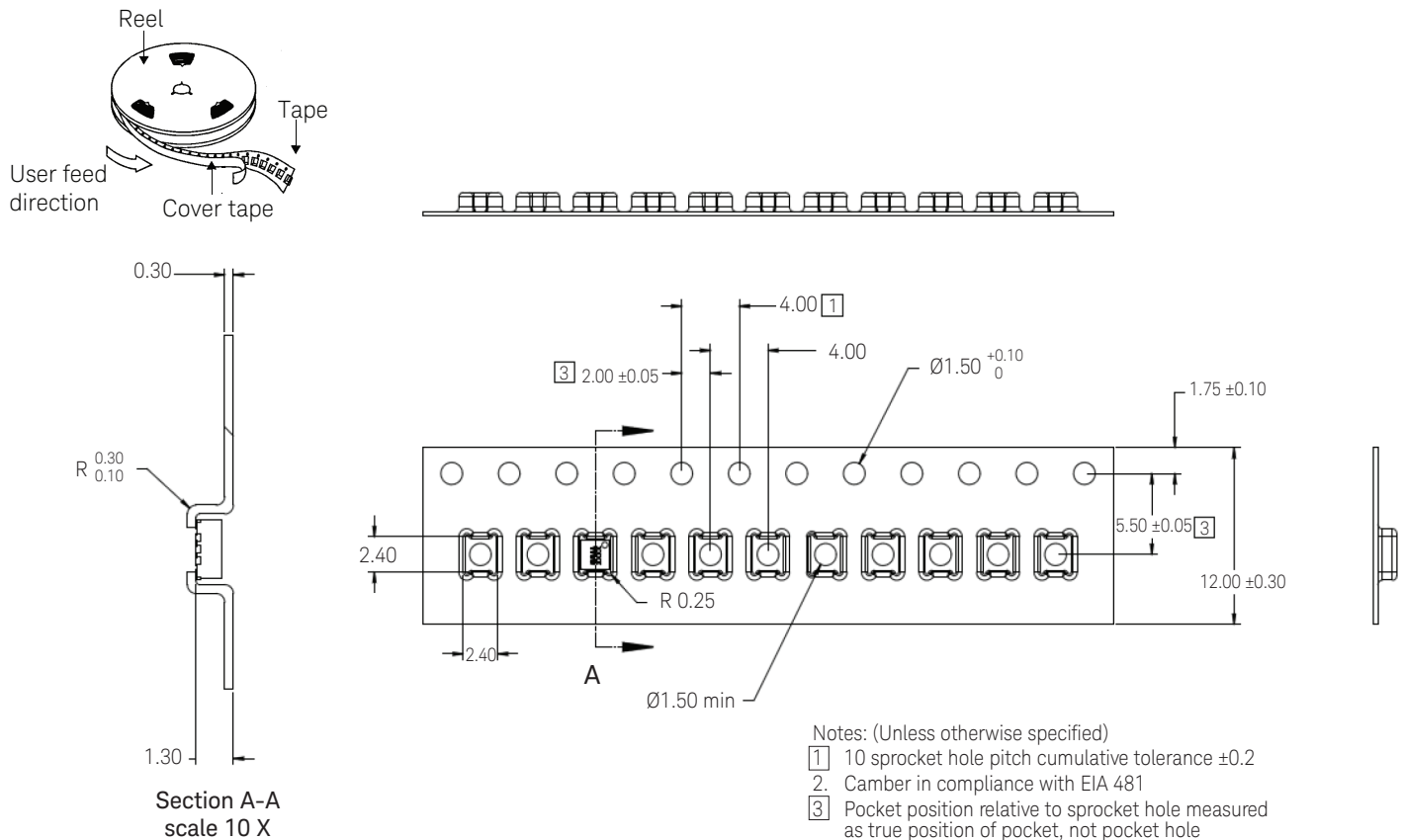


Figure 3. Tape and reel information

## ESD and Handling Precautions

GaAs MMICs in either chip or SMT packages are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

The Keysight Technologies, Inc. document, *GaAs MMIC ESD, Die Attach and Bonding Guidelines*, Application Note (5991-3484EN) provides basic information on these subjects.

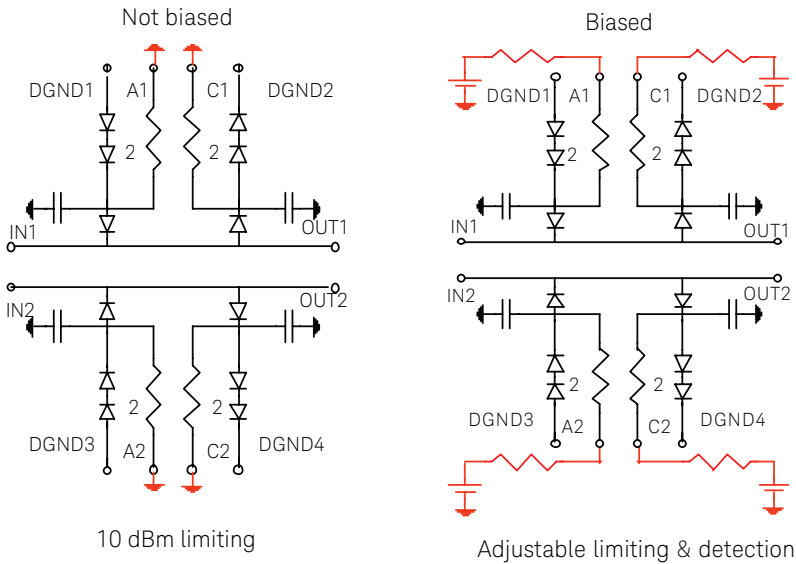


Figure 4. 1GC1-4293 schematic

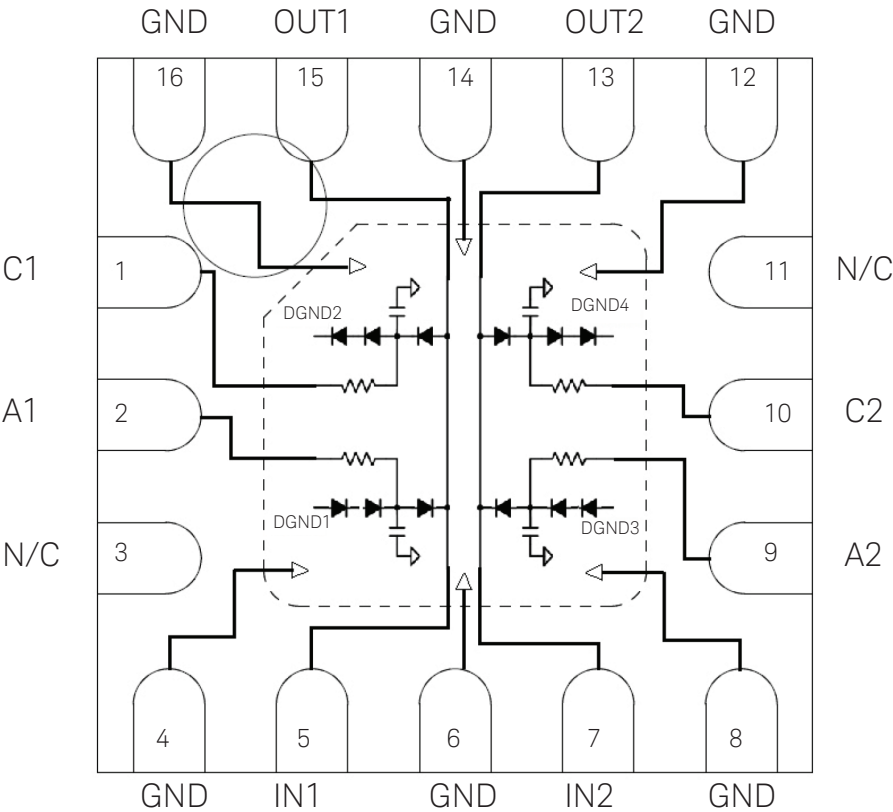


Figure 5. 1GC1-4293 1GC1-4259 pin-out diagram

This footprint is optimized for 10 mil Rogers 4350 layer 1 -2 microstrip width of 20 mils.  
 Exposed vias must be filled and plated over VIPPO recommend 7.9 mils FHS (no solder mask)  
 Use grounded 'area filled' copper on opposite side of the board for proper heatsinking.  
 Use 'area fill' copper (grounded if possible) on layer 1 (shown) and inner layers for additional heatsinking  
 Interconnect layers using ground vias at maximum density (26 mils center to center or 7.9 mil vias) around 10 mm diameter perimeter of part for optimal heatsinking.  
 For footprints compatible with other layer tools, contact MMIC\_Helpline@keysight.com.

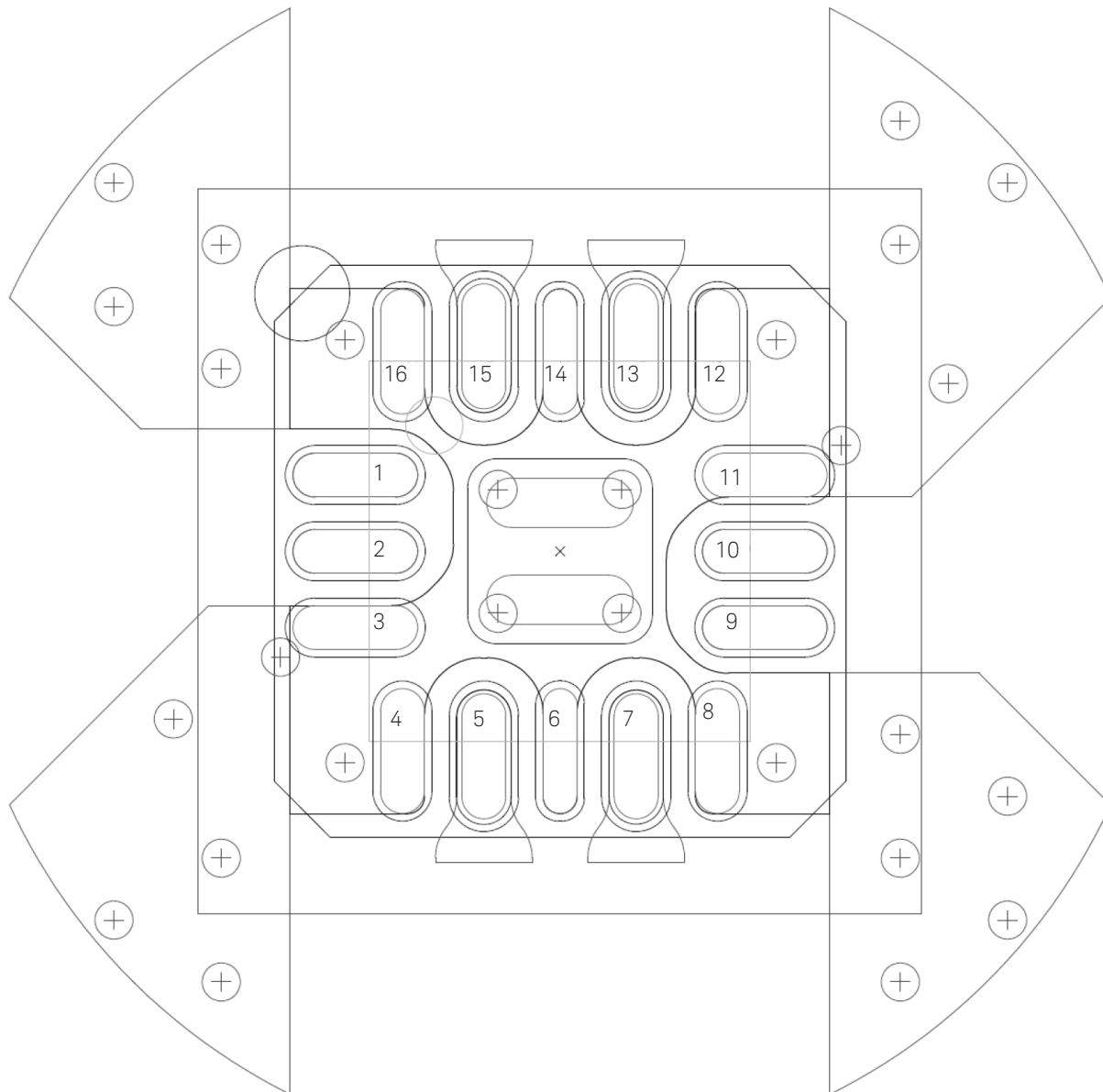


Figure 6. 1GC1-4293 footprint diagram

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The product described in this data sheet is **RoHS Compliant** and **RoHS Process Compatible** with a maximum temperature of 260 °C and a maximum of 3 temperature cycles.

[www.keysight.com/find/mmic](http://www.keysight.com/find/mmic)

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