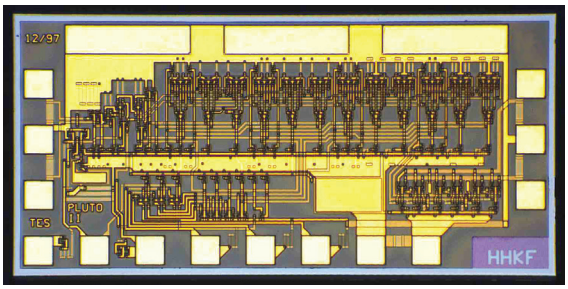
Keysight 1GC1-4021
Broadband GaAs HBT MMIC Multi–Modulus Prescaler

Data Sheet



Features

- Multi–modulus (ECL selectable)
  divide by 1,2,4,8, or 16
- Input frequency range:
  0.1 to 12 GHz (sinewave input)
  DC to 12 GHz (squarewave input)
- High input power sensitivity:
  On–chip pre– and post–amps
  -20 to +10 dBm (Typ. 0.5 to 6 GHz)
  –15 to +10 dBm (Typ. 6 to 10 GHz)
  –10 to +5 dBm (Typ. 10 to 12 GHz
- Dual–mode P_{out}: (chip form)
  0.0 dBm [0.5 V_{p-p}] @ 96 mA
  +6.0 dBm [1.0 V_{p-p}] @ 118 mA
- Low phase noise:
  –153 dBc/Hz @ 100 kHz offset
- (+) or (–) single supply bias op.
- Wide bias supply range:
  4.5 to 6.5 volt operating range
- Differential I/0 with on–chip
  50 Ω matching
- Available in chip form or SSOP
  16–lead surface mount plastic with
  integral heat sink

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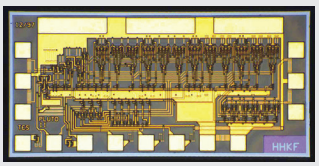
Description

The 1GC1-4021 GaAs HBT MMIC prescaler offers broadband frequency translation for use in communications and EW systems incorporating high–frequency PLL oscillator circuits and signal–path down conversion applications. The prescaler provides multiple–modulus division and input signal pass– through capability as well as a large input sensitivity window, and low phase–noise. The GaAs HBT MMIC prescaler is available in either chip–form (1GC1-4021) or a 16–lead surface– mount plastic package (1GC1-4210). In addition to the features listed above the device offers differential I/O, dual–output power mode plus an input disable contact pad to eliminate any false triggers or self–oscillation condition.



- Chip size: 1470 x 720 µm (57.9 x 28.3 mils)
- Chip size tolerance: ± 10 µm (± 0.4 mils)
- Chip thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
- Pad dimensions: 70 x 70 µm (2.8 x 2.8 mils)

Absolute maximum ratings[1]

(@ TA = 25 °C, unless otherwise indicated)

Symbol	Parameters/conditions	Min	Max	Units
V_{CC}	Bias supply voltage		+7	Volts
V_{EE}	Bias supply voltage	–7		Volts
$\lvert V_{CC} - V_{EE} \rvert$	Bias supply delta		+7	Volts
$V_{A1,A2,A3}$	Modulus select voltage	V_{Logic} –2	V_{CC}	Volts
$V_{Disable}$	Pre–amp disable voltage	V_{EE}	V_{CC}	Volts
V_{Logic}	Logic threshold voltage	V_{CC} –1.5	V_{CC} –1.2	Volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or RF_{in} ports)		V_{CC} ±0.5	Volts
T_{op} [2]	Pkg lead operating temperature	–40	+85	°C
T_{st}	Storage temperature	–65	+165	°C
T_{max}	Maximum assembly temperature (60 seconds max.)		310	°C

1. Operation in excess of any parameter limit (except T_{op}) may cause permanent damage to the device.
2. MTTF >1X10^6 hours @ T_{op} ≤85 °C. Operation in excess of maximum package pin operating temperature (T_{op}) will degrade MTTF.

DC specifications/physical properties

(T_A = 25 °C, V_{CC} – V_{EE} = 5.0 volts, unless otherwise listed)

Symbol	Parameters/conditions	Min	Typ	Max	Units
V_{CC} – V_{EE}	Operating bias supply difference[1]	4.5	5.0	6.5	Volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (HIGH output power configuration[2]: V_{PwrSel} = V_{EE})	100	118	136	mA
	Bias supply current (LOW output power configuration: V_{PwrSel} = open)	83	96	110	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent DC voltage appearing at all RF ports		V_{CC}		Volts
V_{Logic}	Nominal ECL logic level (On–chip, self–biased ECL–threshold voltage)	V_{CC} – 1.40	V_{CC} –1.34	V_{CC} –1.25	Volts

1. Prescaler will operate over full specified supply voltage range. V_{CC} or V_{EE} not to exceed limits specified in absolute maximum ratings section.
2. High output power configuration: $P_{out}[V_{out}]$=+6.0 dBm [1.0V_{p-p}], Low output power configuration: $P_{out}[V_{out}]$= 0.0 dBm [0.5 V_{p-p}].

RF specifications

(T_A = 25 °C, Z_0 = + 50 Ω, V_{CC}–V_{EE} = 5.0 volts)

Symbol	Parameters/conditions	Min	Typ	Max	Units
N_{Ratio}	Divide modulus, N: f_{out}=f_{in}/N, pass–through: N=1		1,2,4,8, or 16		
$f_{in(max)}$	Maximum input frequency of operation[1] (P_{in} = –5 dBm, modulus = 1)	6	8		GHz
	Maximum input frequency of operation (P_{in} = –5 dBm, modulus = ≥2)	12	16		GHz
$f_{in(min)}$	Minimum input frequency of operation[2] (P_{in} = –1 dBm)		0.1	0.3	GHz
$f_{Self-Osc.}$	Output self–oscillation frequency[3]		13.6 / N		GHz
P_{in}	@ DC, (square–wave input)	–20	–25 to > +10	+10	dBm
	@ f_{in}= 500 MHz, (sine–wave input)	–18	–28 to > +10	+10	dBm
	f_{in} = 1 to 4 GHz	–18	–25 to > +10	+10	dBm
	f_{in} = 4 to 6 GHz	–11	–20 to > +10	+9	dBm
	f_{in} = 6 to 10 GHz	–9	–15 to +10	+6	dBm
	f_{in} = 10 to 12 GHz	–7	–10 to +5	+1	dBm
RL	Small–signal input/output return loss (@ f_{in}< 12 GHz)		15		dB
S_{12}	Small–signal reverse isolation (@ f_{in}< 12 GHz)		30		dB
φ_N	SSB phase noise (@ P_{in} = +10 dBm, 100 kHz Offset from a f_{in} = 10.2 GHz carrier, N=2)		–153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in}=10 GHz, P_{in} = –10 dB)		1		pS
T_r or T_f	Edge speed (10% to 90% rise/fall time)		70		pS

1. For output amplitudes with less than 3 dB roll–off from 1 GHz output power values.
2. For sine–wave input signal. Prescaler will operate down to DC for square–wave input signal. Minimum divide frequency limited by input slew–rate.
3. N = Divide modulus. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the pre–amp disable ($V_{Disable}$) feature, or the differential Input de–biasing techniques.

RF specifications (continued)

(T_A = 25 °C, Z_0 = 50 Ω, V_{CC}–V_{EE} = 5.0 volts) **High output power operating mode**[1]

Symbol	Parameters/conditions	Min	Typ	Max	Units
P_{out}	@ f_{out} < 1 GHz,	4.0	6.0		dBm
	@ f_{out} = 3 GHz	3.0	5.5		dBm
	@ f_{out} = 6 GHz	1.0	5.0		dBm
$\|V_{out(p-p)}\|$	@ f_{out} < 1 GHz,		0.99		Volts
	@ f_{out} = 3 GHz		0.94		Volts
	@ f_{out} = 6 GHz		0.88		Volts
$P_{Spitback}$	Output frequency power level appearing at RF_{in} or $\overline{RF}_{in}$ ports. (@ f_{in} 12 GHz, N>1, unused RF_{out} unterminated)		-35		dBm
	Power level of output signal appearing at RF_{in} or $\overline{RF}_{in}$ ports. (@ f_{in} 12 GHz, N>1, Unused RF_{out} terminated into 50 Ω)		-55		dBm
$P_{feedthru.}$	Power level of input signal appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to $P_{in}(f_{in})$, N>1)		25		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to $P_{out}(f_{out})$)		22		dBc
			Low output power operating mode[2]		
P_{out}	@ f_{out} < 1 GHz,		–2.0	0.0	dBm
	@ f_{out} = 3 GHz		–3.0	–0.5	dBm
	@ f_{out} = 6 GHz		–5.0	–1.0	dBm
$\|V_{out(p-p)}\|$	@ f_{out} < 1 GHz,			0.5	Volts
	@ f_{out} = 3 GHz			0.47	Volts
	@ f_{out} = 6 GHz			0.44	Volts
$P_{Spitback}$	Output frequency power level appearing at RF_{in} or $\overline{RF}_{in}$ ports. (@ f_{in} 12 GHz, N>1, unused RF_{out} unterminated)			–45	dBm
	Power level of output signal appearing at RF_{in} or $\overline{RF}_{in}$ ports. (@ f_{in} 12 GHz, N>1, unused RF_{out} terminated into 50 Ω)			–65	dBm
$P_{feedthru}$	Power level of input signal appearing at RF_{out} or $\overline{RF}_{out}$ (@ $f$in = 12 GHz, P_{in} = 0 dBm, referred to $P_{in}(f_{in})$, N>1)			25	dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to $P_{out}(f_{out})$)			22	dBc

1. V_{PwrSel} = V_{EE} .
2. V_{PwrSel} = open circuit.

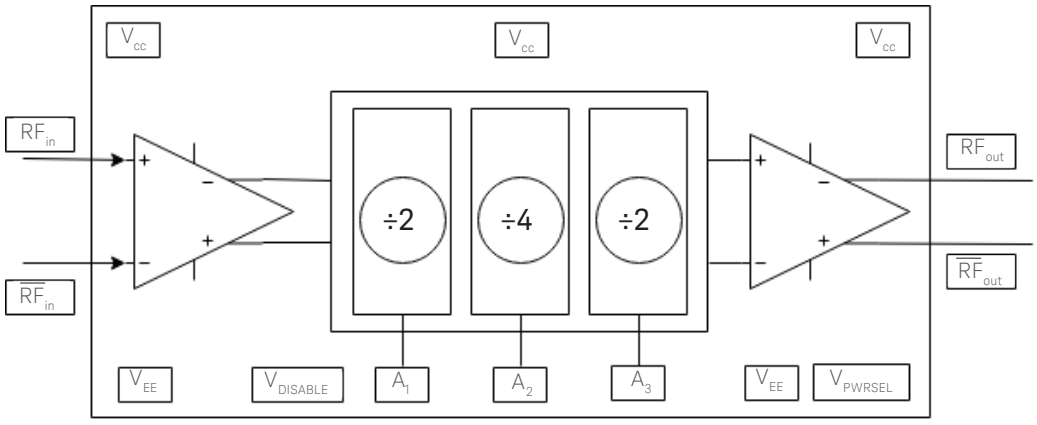


Figure 1. 1GC1-4021 simplified schematic

Applications

The 1GC1-4021 is designed for use in high frequency communications, microwave instrumentation and EW radar systems where low phase–noise PLL control circuitry or broad–band frequency translation is required.

Operation

The device is designed to operate when driven with either a single–ended or differential sinusoidal input signal over a 300 MHz to 12 GHz bandwidth. Below 100 MHz the prescaler input is "slew–rate" limited requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to DC when driven with a square–wave. AC coupling at the RFin lead is recommended for most applications.

The device can be operated from either a single positive or single negative supply. For positive supply operation VCC is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}).

The device will operate in pass–through mode (with unity divide modulus) or at any of four different divide ratios including 2,4,8, or 16 according to following table:

Modulus select truth table

1GC1-4021 **Select lines**[1]

Divide modulus	A_1	A_2	A_3
÷ 1	L	L	L
÷ 2	L	L	H
÷ 4	L	H	L
÷ 8	L	H	H
÷ 16	H	X	X

1. See table valid input logic threshold values

Valid input logic threshold values (ECL–compatible)[1]

(T_A = 25 °C)

Function	Symbol	Conditions	Valid input control levels and resulting current values (volts/mA)
Input disable	$V_{Disble(High)}$ [Disable]		(V_{Logic} + 0.25) through V_{CC}
	$V_{Disable(Low)}$ [Enable]		V_{EE} through (V_{Logic} – 0.25)
	$I_{Disable}$	$V_D > V_{EE}$+3	($V_{Disable}$ –V_{EE} – 3) / 5000
		$V_D < V_{EE}$+3	0
Modulus select	Vselect (A1, A2, A3) (high–state)		(V_{Logic} + 0.25) through V_{CC}
	Vselect (A1, A2, A3) (low–state)		(V_{Logic} –2.0) through (V_{Logic} 0.25)
	Iselect (A1, A2, A3) (high & low–state)		($Vselect_{A1,A2,A3}$–V_{EE} – 3) / 5000

1. See DC specifications table for self–biased V_{Logic} operating values.

Several features are designed onto this prescaler:

Dual–output power feature

Bonding both V_{EE} and V_{PwrSel} pins leads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~ 6.0 dBm [1.0 V_{p-p}] at the RF output port while drawing ~118 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, 0.0 dBm [0.5 V_{p-p}] but at a reduced current draw of ~96 mA resulting in less overall power dissipation.

Note: V_{EE} must *always* be bonded and V_{PwrSel} must *never* be biased to any potential other than V_{EE} or open–circuited.)

V_{Logic} ECL contact pad

Under normal conditions no connection or external bias is required to this pad and it is self–biased to the on–chip ECL logic threshold voltage (V_{CC} – 1.34 V). The user can provide an external bias to this lead (1.5 to 1.2 volts less than VCC) to force the prescaler to operate at a system generated logic threshold voltage.

Input disable feature

By applying an external bias to this pin (more positive than V CC –1.34 V), the input preamplifier stage is locked preventing false trigger frequency division and self–oscillation frequency

Input DC offset

Another method used to prevent false triggers or self–oscillation conditions is to apply a 20 to 100 mV DC offset voltage between the RF_{in} and RF_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

Assembly techniques

Figure 3 shows the chip assembly diagram for single–ended or differential I/O operation through 12 GHz. For positive supply operation, V_{CC} is typically biased to a positive voltage between +4.5 and +6.5 volts and V_{EE} is grounded. For negative supply operation, V_{EE} is typically biased between –4.5 to –6.5 volts and V_{CC} is grounded. In either case the supply contact to the chip must be capacitively bypassed (50 to 200 pF, recommended) to provide good input sensitivity and low input power feedthrough. All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor (>400 pF) must be added to provide proper RF bypassing.

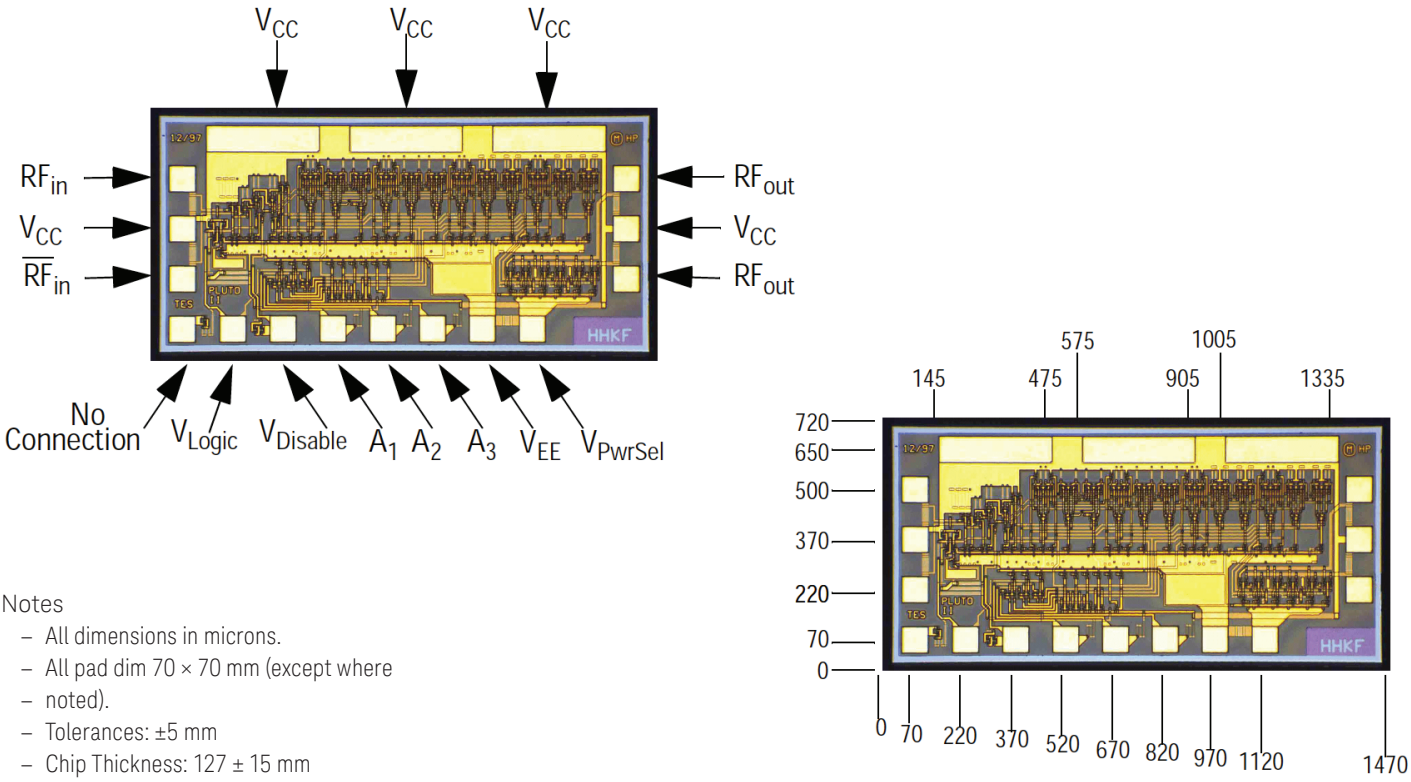
Since the voltage applied to the modulus select lines must not be less than V_{Logic} – 2.0 volts, 2 KΩ resistors are generally added between the select line controls and the V_{EE} supply rail. In general, AC coupling capacitors are recommended on the RF_{in} and RF_{out} connections to the device. For positive supply operation, V_{CC} is positively biased resulting in a positive DC voltage appearing at RF_{in} or RF_{out}. In this case a AC coupling cap is required.

Due to on–chip 50Ω matching resistors at all four RF ports, no external termination is required. However, improved input sensitivity and reverse "Spitback" performance (~15 dB) can be achieved by terminating the unused RFout port to V_{CC} through 50 Ω or to ground through an AC coupling capacitor (positive supply operation) or to ground via a 50 Ω termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Keysight Technologies, Inc. document, *GaAs MMIC ESD, Die Attach and Bonding Guidelines, Application Note* (5991-3484EN).



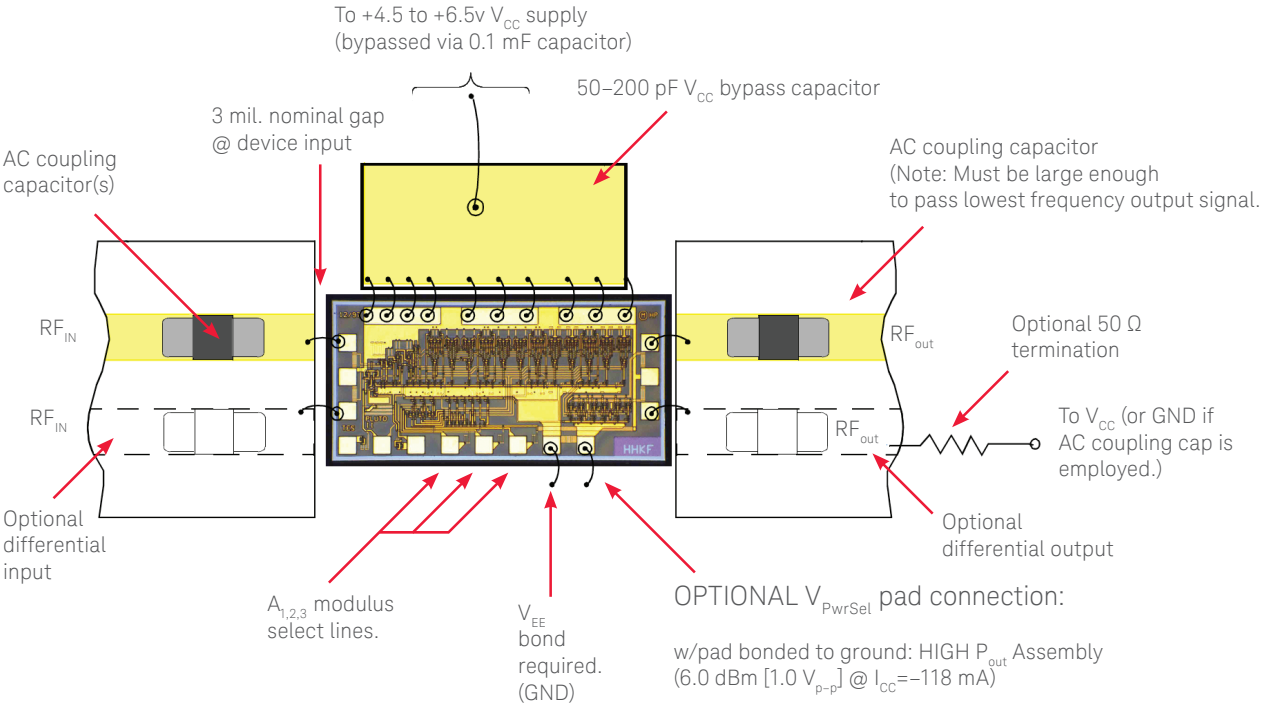
Notes
- All dimensions in microns.
- All pad dim 70 × 70 mm (except where
- noted).
- Tolerances: ±5 mm
- Chip Thickness: 127 ± 15 mm

Figure 2. Pad Location and Chip Dimensions

RoHS Compliance

The 1GC1-4262 prescaler is RoHS Compliant. This means the component meets the requirements of the European Parliament and the Council of the European Union Restriction of Hazardous Substances Directive 2011/65/EU, commonly known as RoHS. The six regulated substances are lead, mercury, cadmium, chromium VI (hexavalent), polybrominated biphenyls (PBB) and polybrominated biphenyl ethers (PBDE). RoHS compliance implies that any residual concentration of these substances is below the RoHS Directive's maximum concentration values (MVC); being less than 1000 ppm by weight for all substances except for cadmium which is less than 100 ppm by weight.

Positive supply



Negative supply

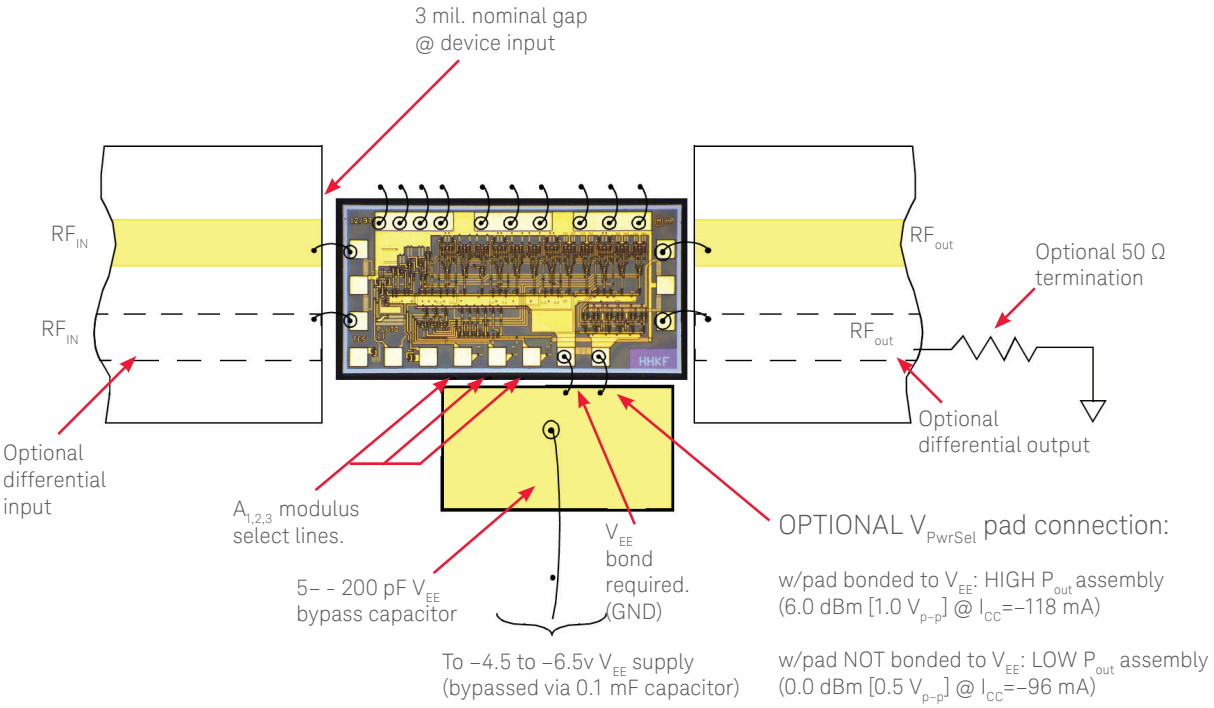


Figure 3. Assembly diagrams

Supplemental Data

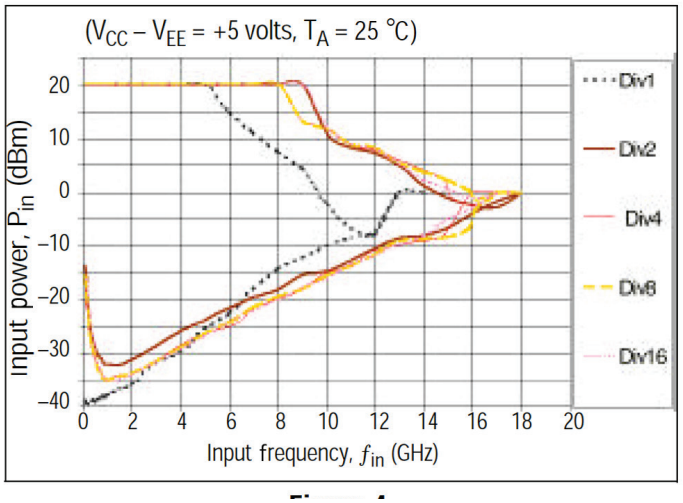


Figure 4. Input sensitivity window

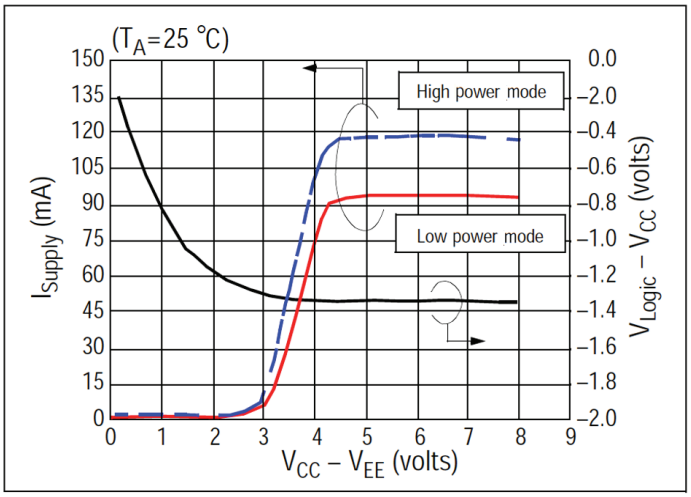


Figure 5. Supply current & V_{Logic} vs. supply voltage

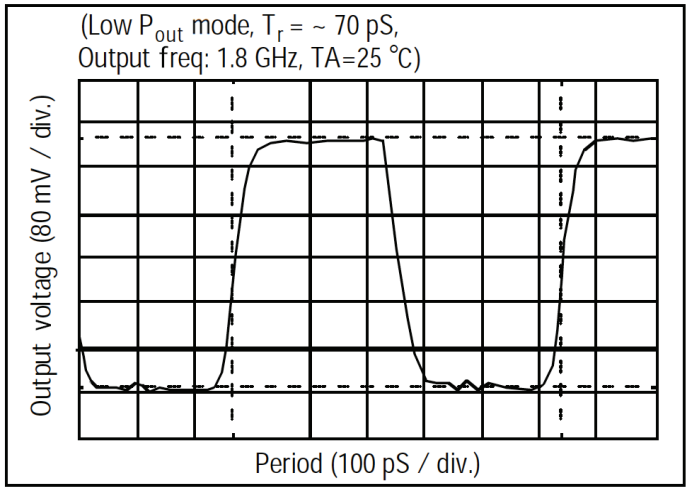


Figure 6. Output voltage waveform (low P_{out} mode)

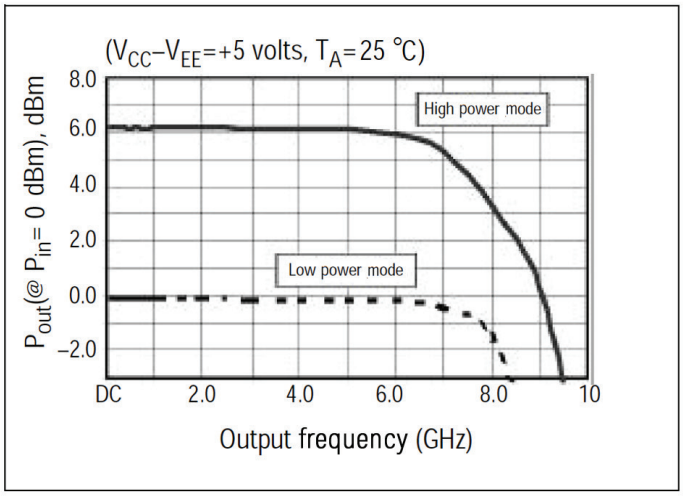


Figure 7. Output power vs. output frequency, f_{out} (GHz)

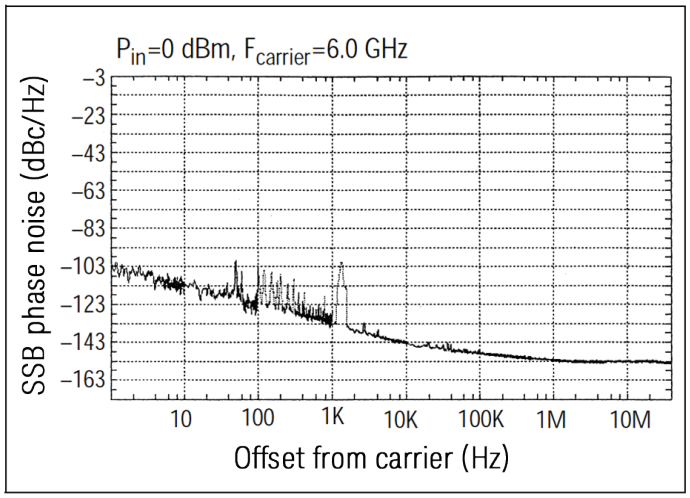


Figure 8. Phase noise performance

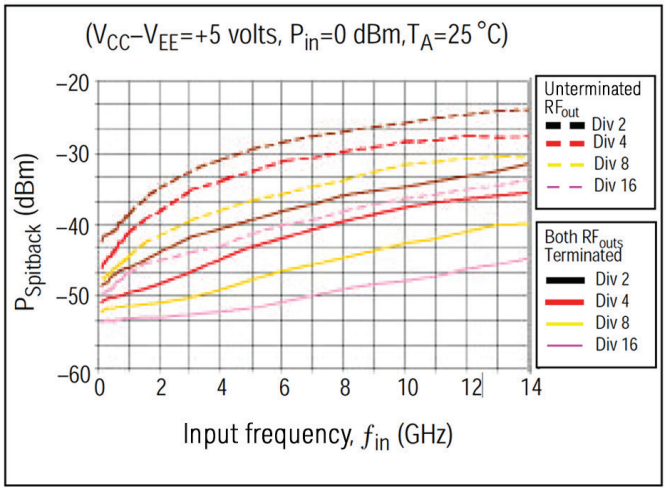


Figure 9. "Spitback" power P(f_{ou}) appearing at RF input port

Supplemental Data

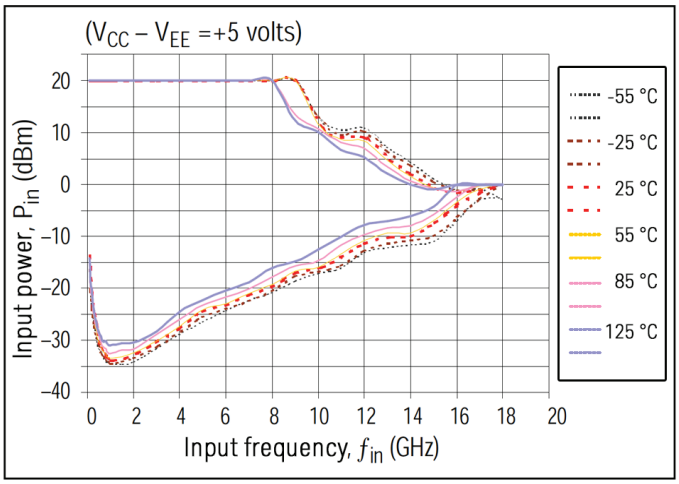


Figure 10. Typical divide–by–2 input sensitivity window (over temperature)

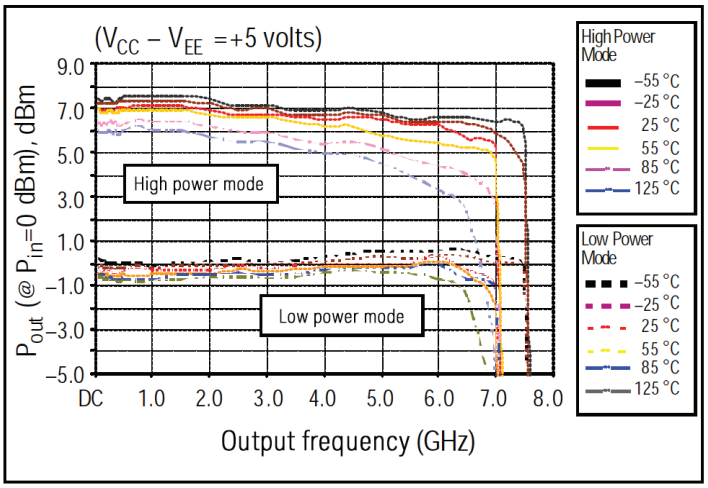


Figure 11. Typical divide–by–2 output power vs. output frequency (over temperature)

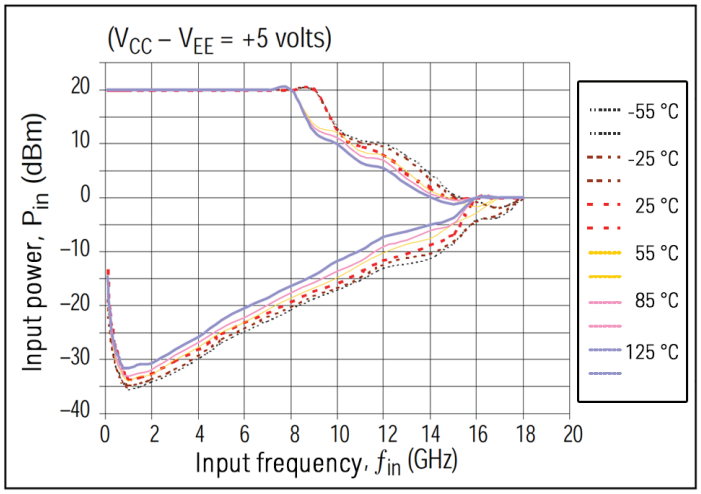


Figure 12. Typical divide-by-16 input sensitivity window (over temperature)

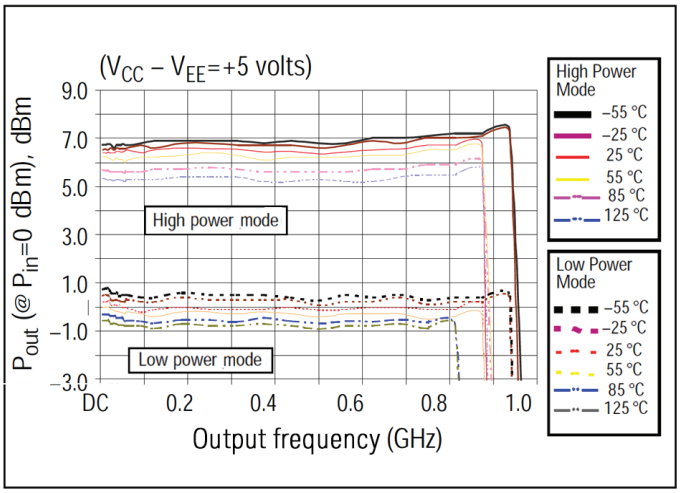


Figure 13. Typical divide-by-16 output power vs. output frequency (over temperature)

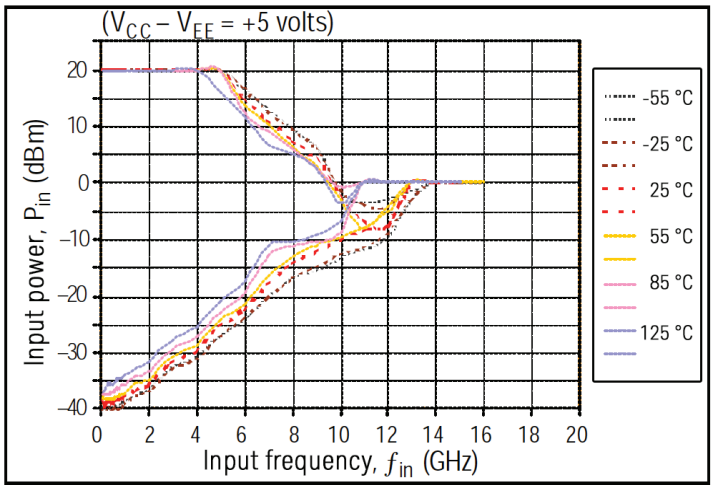


Figure 14. typical pass–through input sensitivity window (over temperature)

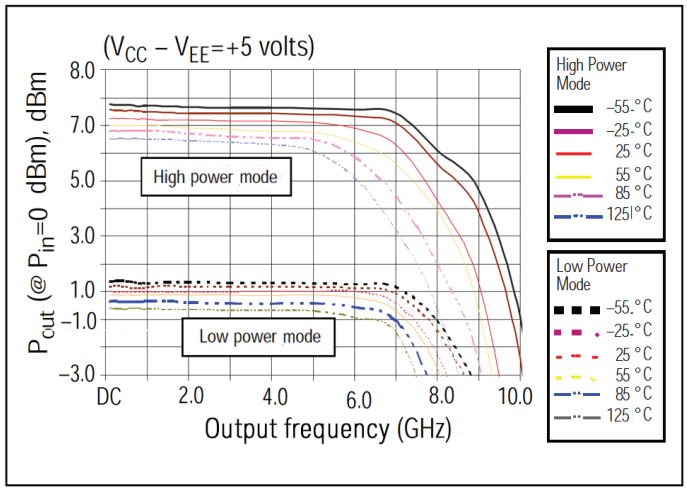
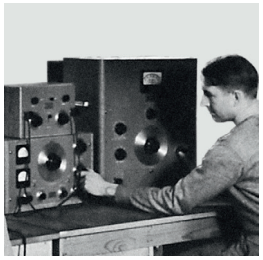
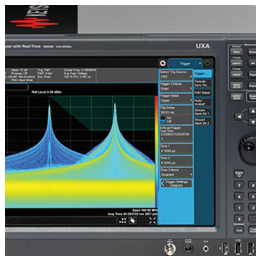


Figure 15. Typical pass–through output power vs. output frequency (over temperature)

Evolving

Our unique combination of hardware, software, support, and people can help you reach your next breakthrough. We are unlocking the future of technology.





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The product described in this data sheet is RoHS Compliant and RoHS Process Compatible with a maximum temperature of 260 °C and a maximum of 3 temperature cycles.

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