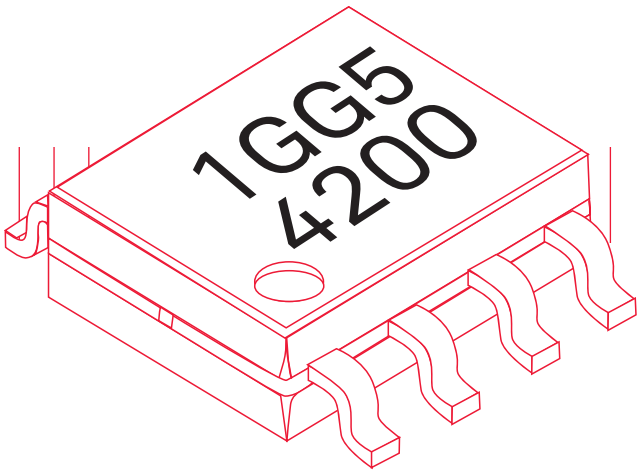
Keysight 1GG5-4200
DC - 5 GHz SMT Packaged GaAs Diode Limiter

Data Sheet



Features

- High forward voltage:
  4.1V typ. @ 1 mA
- Good return loss:
  < –18 dB typ. to 5 GHz
- Low insertion loss:
  < 0.7 dB typ. @ 2 GHz
  < 1.0 dB typ. @ 4 GHz
- P_{-1dB}: 26 dBm typ.
- Distortion:
  SHI: +100 dBm typ.
  THI: +53 dBm typ.
  TOI: +50 dBm typ.

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Description

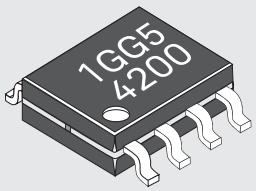
The 1GG5-4200 is a packaged 5 GHz reverse power protection (RPP) and limiter GaAs ID. The device can be used to protect sensitive RF circuits from excess RF power, DC transients and ESD from DC to 5 GHz. The circuit contains Planar–Doped–Barrier (PDB) diodes with integrated matching networks consisting of spiral inductors and MIM capacitors. The device is fabricated with the Modified Barrier Integrated Diode (MBID) process. This process allows the barrier height of the diodes and the number of diodes in each "stack" to be optimized for low harmonic distortion when P_{in} < 20 dBm while limiting transmitted power to less than 1 watt when P_{in} = 10 watts.

Absolute maximum ratings[1]

(@ T_A = 25 °C, unless otherwise indicated)

Symbol	Parameters/conditions	Min	Max	Units
P_{cont}	Maximum continuous RF input power		4 (36)	Watts (dBm)
I_{cont}	Maximum continuous DC current		160	mA
T_{op}	Operating temperature	–55	+125	°C
T_{st}	Storage temperature	–65	+165	°C
T_{max}	Max. assembly temperature		+240	°C

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25 °C except for T_{op}, T_{st}, and T_{max}.



- Package type: 8–lead SOIC8 plastic w/heat–slug
- Package dimensions: 4.93 × 3.94 mm (0.194 × 0.155 in) w/o leads
- Package thickness: 1.473 mm (0.060 in) typ.
- Lead pitch: 1.27 mm (0.050 in) nom.
- Lead width: 0.25 mm (0.010 in) nom.

Applications

The 1GG5-4200 was designed for reverse power protection (RPP), limiter and ESD protection applications. When used as a shunt limiter, 1 dB compression occurs when P_{in} = ~25 dBm and small–signal insertion loss is less than 1 dB up to 6 GHz. The 1GG5-4200 can also protect sensitive components from ESD damage. The degree of protection offered is dependent on the protected component's characteristics. ESD damage level for the 1GG5-4200 by itself is greater than 8 kv (measured with IEC801–2, 150 pF, 330 ohm ESD generator).

Biasing and Operation

The 1GG5-4200 needs no bias.

Assembly Techniques

This package is compatible with SMT assembly processes. The leads and backside are tin plated to facilitate soldering.

Diodes are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

Diode ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful diode performance and reliability.

Keysight document, *GaAs MMIC ESD, Die Attach and Bonding Guidelines - Application Note* (5991-3484EN) provides basic information on these subjects.

Moisture sensitivity classification: Class 1, per JESD22-A112-A.

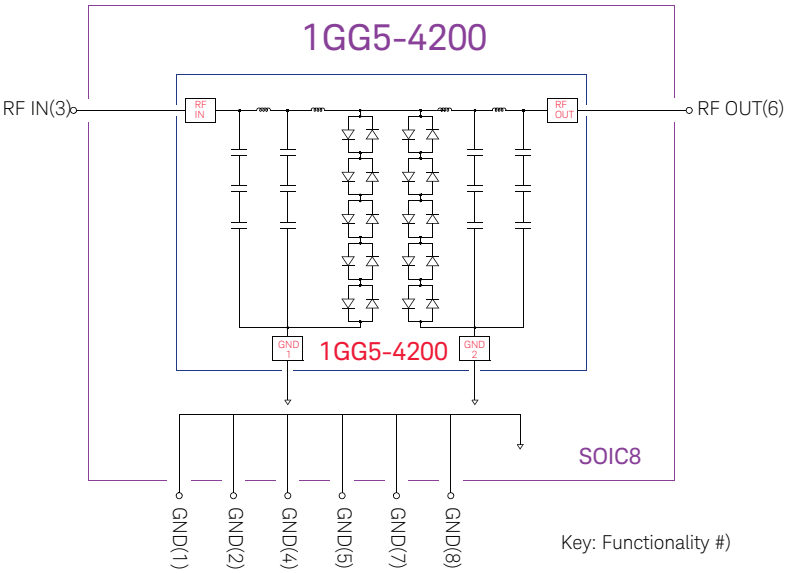
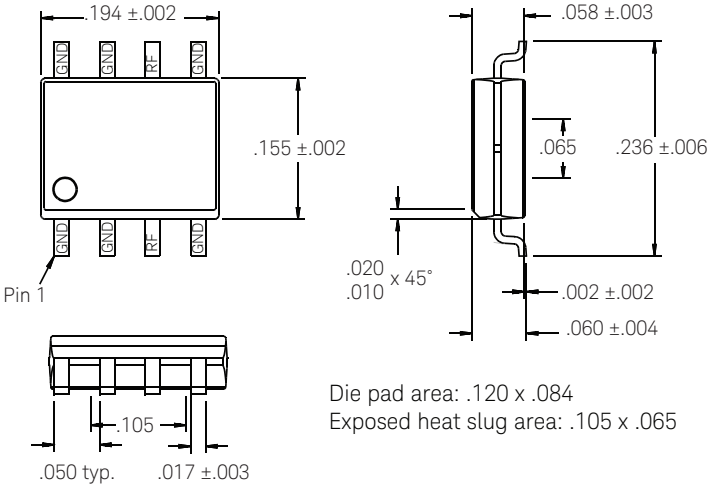
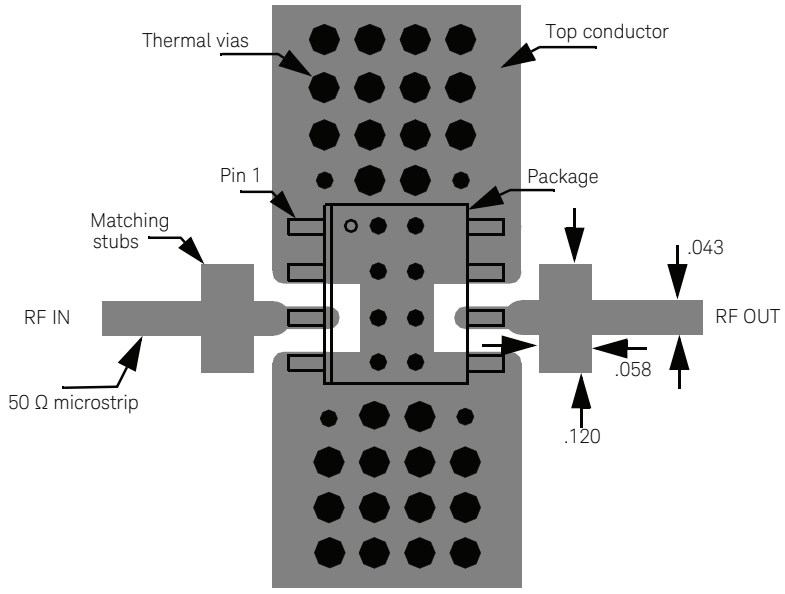


Figure 1. 1GG5-4200 schematic



Notes
1. All dimensions in inches.
2. Refer to JEDEC Outline MS-012 for additional tolerances.

Figure 2. 1GG5-4200 package outline drawing



Notes
1. All dimensions in inches.
2. Matching stubs required above 2 GHz.
3. Power dissipation is critical.
4. Top conductor ground plane pattern should be used on all inner PCB layers.

Figure 3. 1GG5-4200 PCB layout (.021" GETEK)

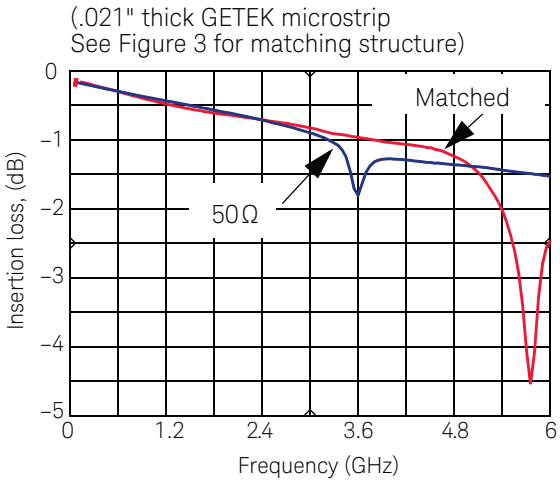


Figure 4. Typical insertion loss vs. frequency

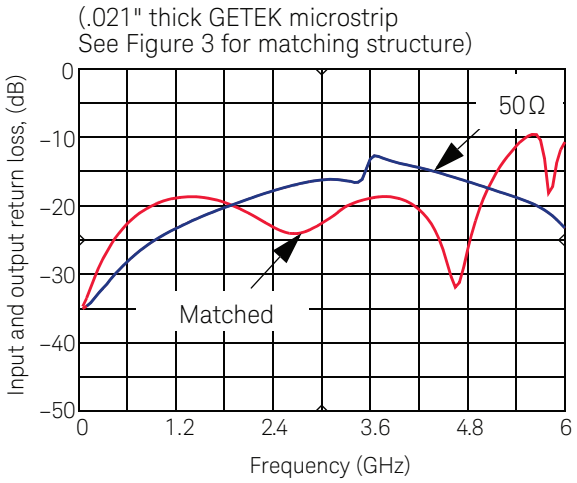


Figure 5. Typical input return loss vs. frequency

Typical S–parameters

(T_{amb}= 25 °C, mounted on .021" GETEK microstrip, no matching)

Freq (GHz)	S_{11},S_{22}			S_{21},S_{12}		
	dB	Mag	Ang	dB	Mag	Ang
0.05	–35.031	0.018	–6.669	–0.163	0.981	–6.876
0.10	–34.638	0.019	–14.266	–0.174	0.980	–13.637
0.5	–29.343	0.034	–63.313	–0.273	0.969	–67.198
1.0	–24.584	0.059	–95.831	–0.392	0.956	–133.649
1.5	–21.662	0.083	–115.891	–0.501	0.944	159.932
2.0	–19.412	0.107	–133.924	–0.615	0.932	93.422
2.5	–17.463	0.134	–154.948	–0.744	0.918	26.422
3.0	–16.205	0.155	–178.590	–0.901	0.901	–40.554
3.5	–16.140	0.156	176.807	–1.445	0.847	–109.422
4.0	–13.887	0.202	134.809	–1.275	0.863	–172.647
4.5	–15.365	0.171	109.780	–1.329	0.858	119.404
5.0	–17.203	0.138	88.365	–1.384	0.853	50.951
5.5	–19.198	0.110	77.813	–1.457	0.846	–18.514
6.0	–23.222	0.069	91.195	–1.530	0.838	–89.272

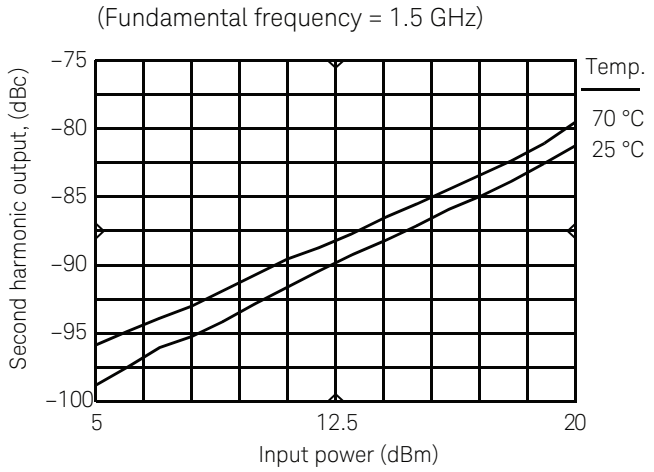


Figure 6. Typical second harmonic performance vs. Temperature

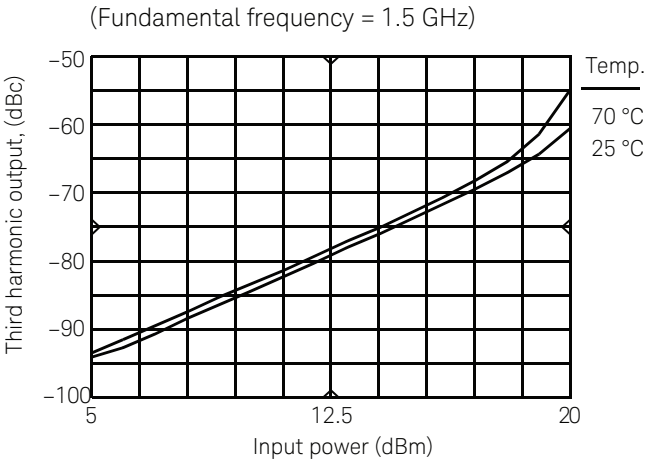


Figure 7. Typical third harmonic performance vs. Temperature

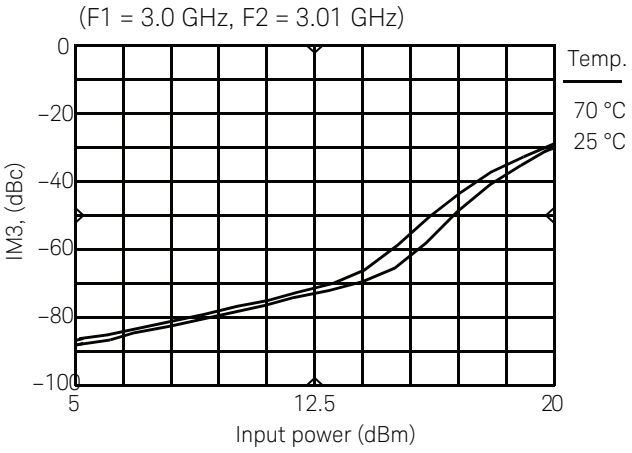


Figure 8. Typical third order intermodulation vs. Temperature

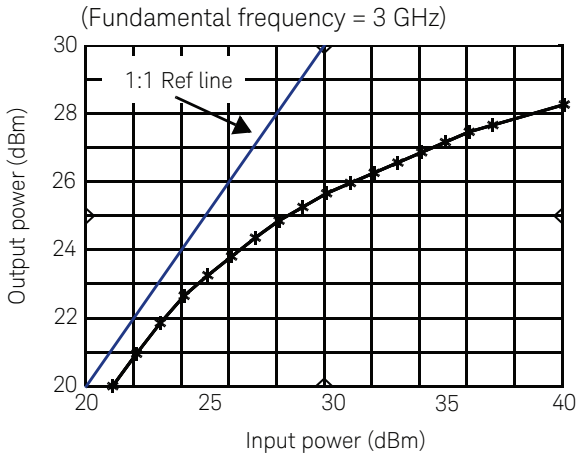


Figure 9. Typical P_{out} vs. P_{in}

1. All data measured on individual devices mounted in test package @ T_A = 25 °C (except where noted).
2. This data sheet contains a variety of **typical** and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. Customers considering the use of this, or other HFTC GaAs ICs, for their design should obtain the current production specifications from HFTC Marketing. In this data sheet the term typical refers to the 50th percentile performance.

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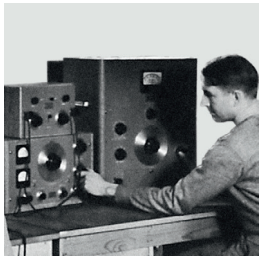

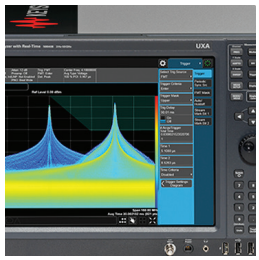

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Published in USA, August 26, 2016
5992-1743EN
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