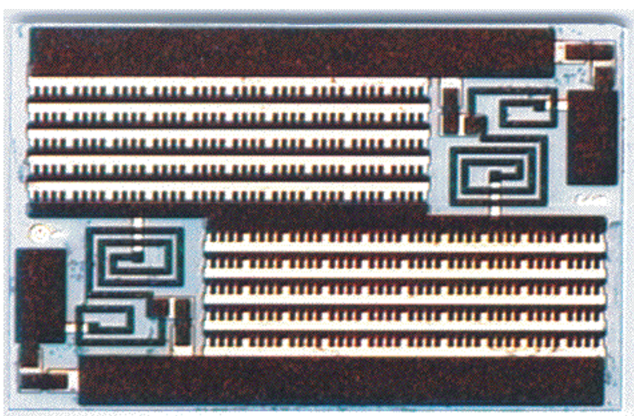
Keysight Technologies

6 GHz Integrated GaAs Diode Limiter

1GG5-4028



Data Sheet

Features

- High forward voltage:
  4.1V Typ. @ 1 mA
- Good port match:
  S11 < –18 dB typ.
  S22 < –18 dB typ.
- Low insertion loss:
  <0.5 dB typ. @ 3 GHz
  <0.8 dB typ. @ 6 GHz
- P-1dB: 26 dBm typ.
- Distortion:
  SHI: +100 dBm typ.
  THI: +53 dBm typ.
  TOI: +50 dBm typ.

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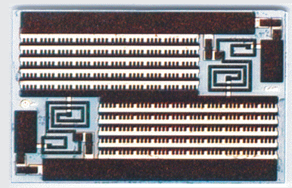
Description

The 1GG5-4028 is a 6 GHz reverse power protection (RPP) and limiter GaAs ID. The device can be used to protect sensitive RF circuits from excess RF power, DC transients and ESD from DC to 6 GHz. The circuit contains planar–doped–barrier (PDB) diodes with integrated matching networks consisting of spiral inductors and MIM capacitors. The device is fabricated with the modified barrier integrated diode (MBID) process. This process allows the barrier height of the diodes and the number of diodes in each “stack” to be optimized for low harmonic distortion when P in < 20 dBm while limiting transmitted power to less than 1 watt when P_{in} = 10 watts.



- Chip size: 1310´ 860 mm (51.6´ 33.7 mils)
- Chip size tolerance: ± 10 mm (± 0.4 mils)
- Chip thickness: 127 ± 15 mm (5.0 ± 0.6 mils)
- RF pad dimensions: 175´ 80 mm (6.9´ 3.1 mils), or larger

Absolute maximum ratings[1]

(@ T_A = 25 °C, unless otherwise indicated)

Symbol	Parameters/conditions	Min	Max	Units
P_{cont}	Maximum continuous RF input power		5 (37)	Watts (dBm)
I_{cont}	Maximum continuous DC current		160	mA
T_j	Junction temperature		150	°C
Top	Operating temperature	–55	100	°C
T_{st}	Storage temperature	–65	+165	°C
T_{max}	Max. assembly temperature		300	°C

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{ch}, T_{stg}, and T_{max}.

Applications

The 1GG5-4028 was designed for reverse power protection (RPP), limiter and ESD protection applications. When used as a shunt limiter, 1 dB compression occurs when P_{in} = ~25 dBm and small–signal insertion loss is less than 1 dB up to 6 GHz. The 1GG5-4028 can also protect sensitive components from ESD damage. The degree of protection offered is dependent on the protected component’s characteristics. ESD damage level for the 1GG5-4028 by itself is greater than 8 kv (measured with IEC801–2, 150 pF, 330 ohm ESD generator).

Biasing and operation

The 1GG5-4028 needs no bias.

Assembly techniques

Epoxy die–attach using conductive epoxy or solder die–attach using a fluxless AuSu solder preform can be used for assembly. Gold thermosonic wedge bonding with 0.7 mil diameter Au wire is recommended for all bonds. Tool force should be 22 ± 1 gram, stage temperature should be 150 ± 2°C, and ultrasonic power and duration should be 64 ± 1 dB and 76 ±8 msec, respectively. The bonding pad and chip backside metallization is gold.

Diodes are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. Diode ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful diode performance and reliability.

Keysight document, “*GaAs MMIC ESD, Die Attach and Bonding Guidelines - Application Note*” (5991-3484EN) provides basic information on these subjects.

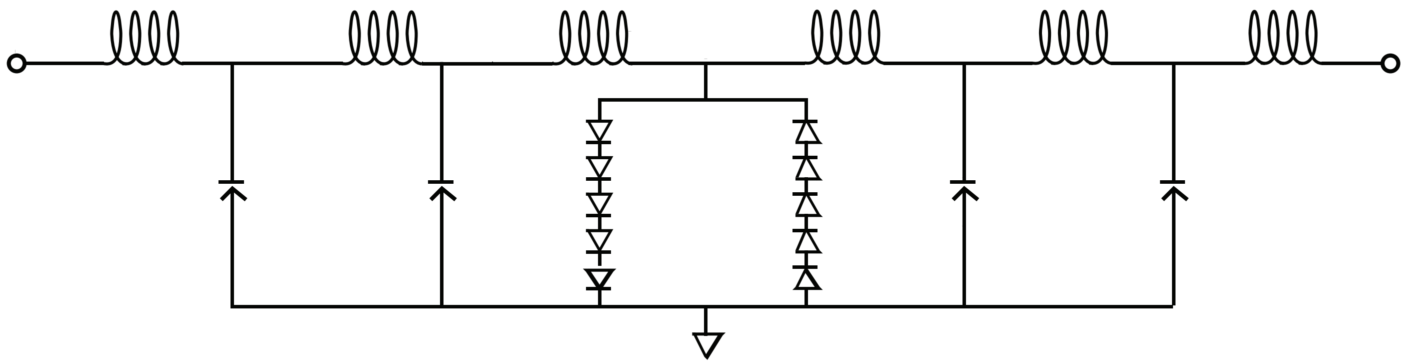
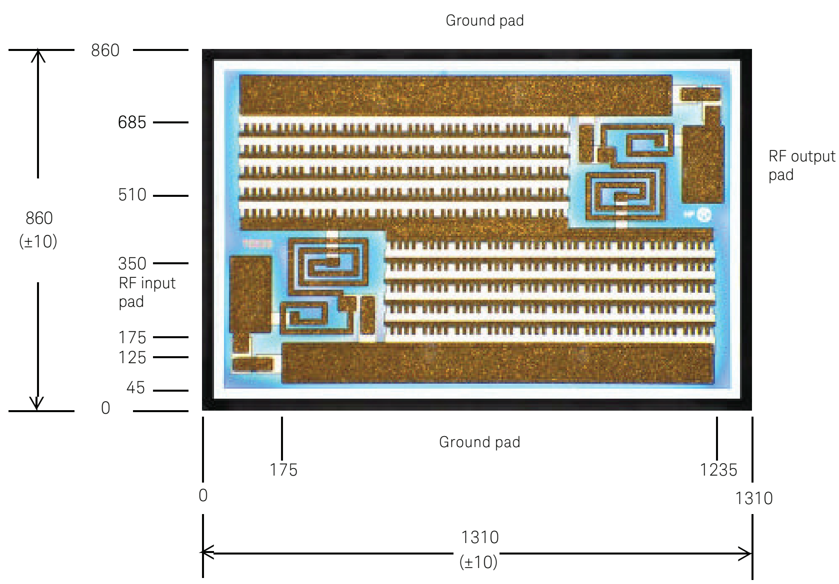


Figure 1. 1GG5-4028 schematic



1. All dimensions in microns.
2. RF pad dim.: 175´80 mm.
3. All other dimensions: ± 5 mm (unless otherwise noted).
4. Chip thickness: 127 ± 15 mm.

Figure 2. 1GG5-4028 bond pad locations

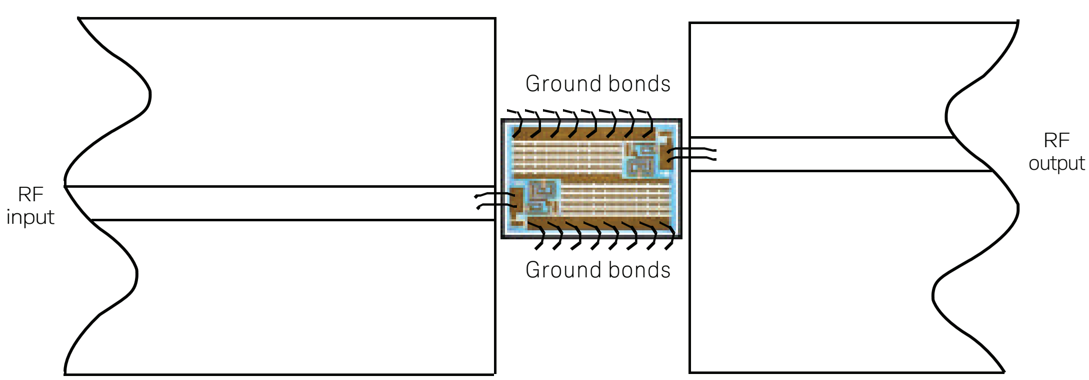


Figure 3. 1GG5-4028 assembly diagram

(Input and output bond wire inductance = 0.3 nH)

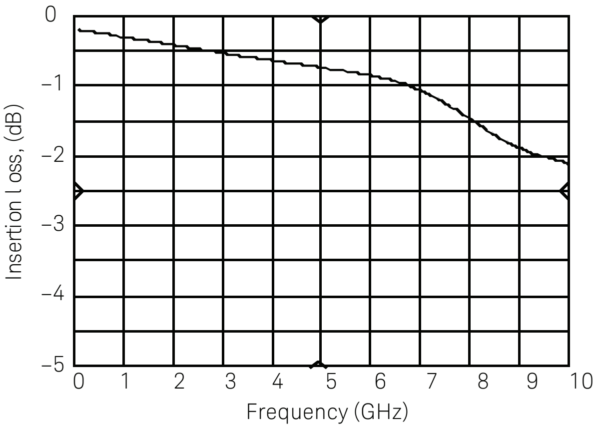


Figure 4. Typical insertion loss vs. frequency

(Input and output bond wire inductance = 0.3 nH)

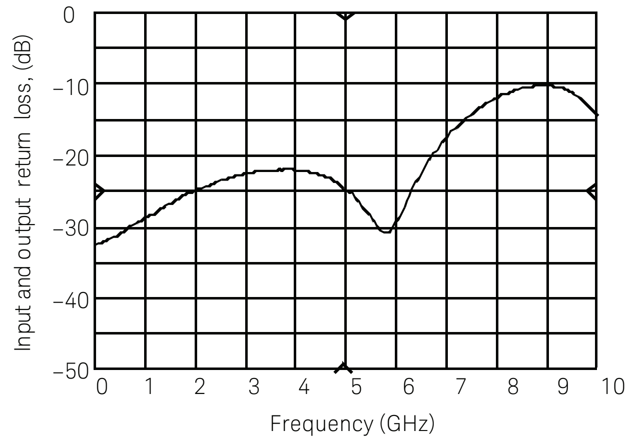


Figure 5. Typical input and output return loss vs. frequency

Typical S–parameters

(T_{chuck} = 25 °C, input and output bond wire inductance = 0.3 nH)

Freq (GHz)	S11,S 22			S21,S12		
	dB	Mag	Ang	dB	Mag	Ang
0.05	–32.221	0.024	–2.241	–0.228	0.974	–1.459
0.10	–32.144	0.025	–4.121	–0.227	0.974	–2.888
0.5	–30.746	0.029	–26.764	–0.263	0.970	–14.254
1.0	–28.664	0.037	–57.231	–0.322	0.964	–28.226
1.5	–26.618	0.047	–83.770	–0.373	0.958	–42.135
2.0	–24.730	0.058	–108.166	–0.436	0.951	–56.078
2.5	–23.303	0.068	–129.362	–0.490	0.945	–70.058
3.0	–22.260	0.077	–148.565	–0.548	0.939	–84.101
3.5	–21.710	0.082	–165.969	–0.606	0.933	–98.320
4.0	–21.662	0.083	178.983	–0.652	0.928	–112.776
4.5	–22.273	0.077	165.600	–0.707	0.922	–127.450
5.0	–24.141	0.062	156.143	–0.757	0.917	–142.440
5.5	–27.835	0.041	160.793	–0.798	0.912	–157.782
6.0	–28.899	0.036	–146.270	–0.874	0.904	–175.401
6.5	–22.176	0.078	–126.263	–0.961	0.895	168.026
7.0	–17.240	0.137	–132.438	–1.093	0.882	150.845
7.5	–13.903	0.202	–144.972	–1.271	0.864	133.106
8.0	–11.640	0.262	–159.638	–1.495	0.842	114.903
8.5	–10.318	0.305	–174.971	–1.720	0.820	96.133
9.0	–9.959	0.318	169.854	–1.910	0.803	76.497
9.5	–10.953	0.283	156.718	–2.028	0.792	55.121
10.0	–14.404	0.190	156.832	–2.155	0.780	30.458

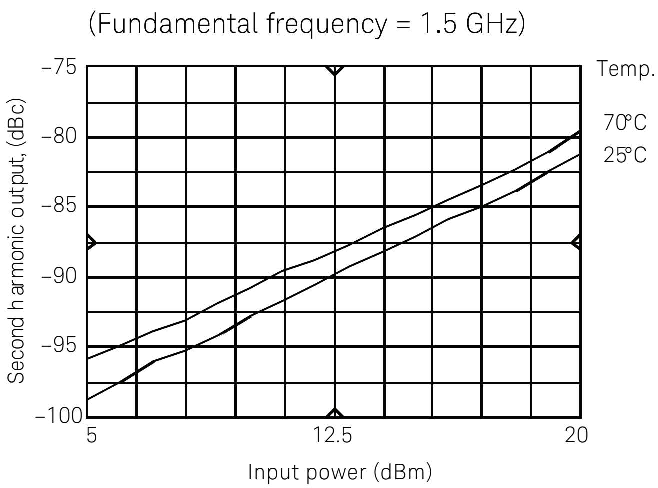


Figure 6. Typical second harmonic performance vs. temperature

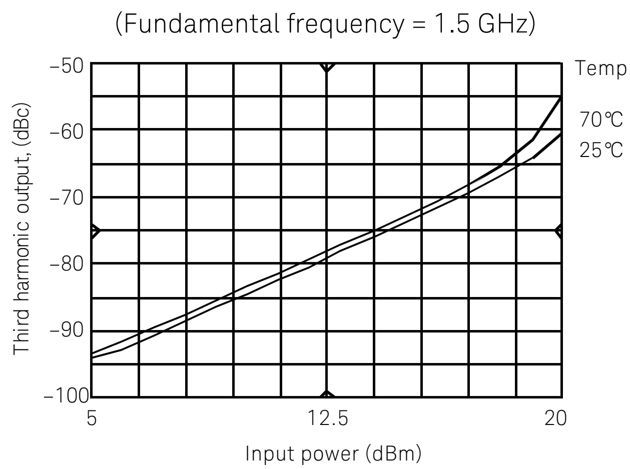


Figure 7. Typical third harmonic performance vs. temperature

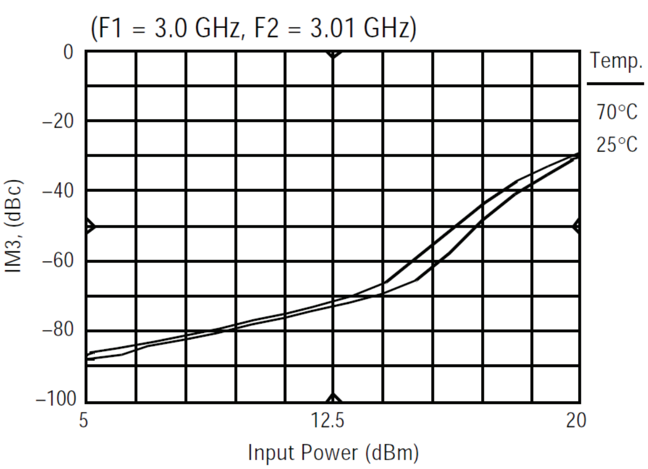


Figure 8. Typical third order intermodulation vs. temperature

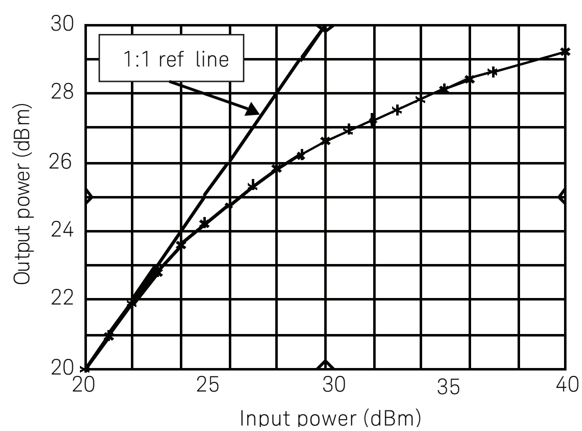


Figure 9. Typical P_{out} vs. P_{in}

1. All data measured on individual devices mounted in test package
2. @ T_A = 25 °C (except where noted).
3. This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications.

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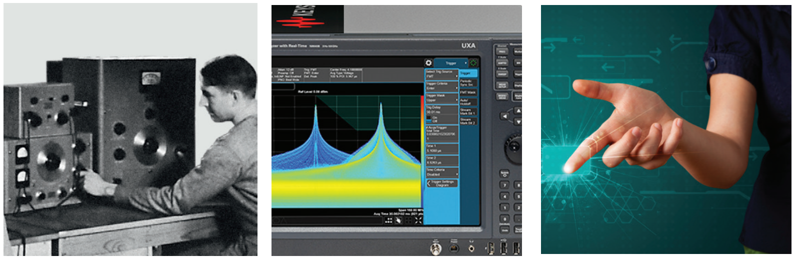

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Published in USA, August 22, 2016
5992-1741EN
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