M9703B

AXIe high-speed digitizer / wideband digital receiver
8 channels, 12-bit, up to 3.2 GS/s,
DC up to 2 GHz bandwidth

Introduction

The M9703B is a very fast versatile DC-coupled 12-bit wideband digital receiver/digitizer, providing exceptional measurement fidelity over multiple phase-coherent channels. Based on the AXIe standard, offering eight acquisition channels in a single-slot card, it provides excellent channel density and flexible scalability. These features allow the implementation of a large number of high dynamic range, phase-coherent channels in a small volume, making the M9703B ideal for multi-channel applications in advanced physics, aerospace & defense, and RF communications with adjustable center frequency and analysis bandwidth.

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Overview

Product Description

The M9703B is an 8-channel, 12-bit wideband digital receiver/digitizer, with a patented front-end that is able to capture signals from DC up to 2 GHz[1] at 1.6 GS/s, with exceptional measurement accuracy. An interleaving capability allows two channels to be combined to acquire at 3.2 GS/s on four channels, with up to 1.4 GHz instantaneous bandwidth.

The M9703B also provides up to 16 GB of DDR3 acquisition memory and real-time data processing capability with four Xilinx Virtex-6 FPGAs.

The on-board FPGAs can feature an optional real-time digital down-converter (DDC) that allows tuning and zooming on the signal to be analyzed. This DDC functionality improves the dynamic range, reduces the noise floor, extends the capture time, and accelerates measurement speed.

The M9703B can also be combined with the Keysight PathWave VSA Software and Keysight U1092A Multichannel Acquisition Software for advanced multichannel signal analysis.

Example Applications

- Advanced research experiments, such as hydrodynamics or plasma fusion
- Radar and satellite communication applications, such as antenna array calibration/test, passive radar receiver, or multi-band SATCOM monitoring
- Emerging standards (5G) R&D & DVT in massive MIMO, or multichannel baseband IQ

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1. 2 GHz refers to the front-end bandwidth. The digitizer can operate in the 1st and 2nd Nyquist zones (using undersampling), but real-time bandwidth is limited by Nyquist to a maximum of [sampling rate/2], capped by the bandwidth option.

Product Features

- 12-bit ADC resolution
- 8 channels (4 when interleaving with -INT option)
- Up to 3.2 GS/s sampling rate (with -SR2 and -INT options)
- DC up to 2 GHz input frequency range (with -F10 option in non-interleaved mode)
- Up to 16 GB (1 GSamples/ch) of DDR3 acquisition memory
- 50 Ω input impedance, DC coupled
- Selectable 1 V or 2 V full scale range (FSR)
- ±2x FSR input voltage offset range
- ±200 fs channel-to-channel skew stability
- Up to 15 ps RMS trigger time interpolator (TTI) precision (with -SR2 option)
- Enhanced real-time processing using configurable Xilinx Virtex-6 FPGAs[1]
- PCIe four lanes (x4) backplane for up to 1.4 GB/s sustained data throughput
- Real-time digital down-conversion (-DDC option) on 8 phase-coherent channels
- Real-time digital down-conversion with I/Q streaming and recording bundles (-CB1 and -CB2)
- Support for Windows and Linux

Uncompromising Values

- Very wide bandwidth and fast acquisition with optimized dynamic range
- Scalable phase-coherent acquisition channels in a small space
- High measurement throughput
- Reduced test time by tuning and zooming on signals (-DDC option):
    - Isolate the signal of interest
    - Improve the dynamic range
    - Extend the capture time, or reduce the amount of transferred data
    - Trigger on the signal of interest
- Multichannel phase coherent streaming and recording measurements with up to 320 MHz alias protected instantaneous bandwidth (IBW) via bundles -CB1 and -CB2

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1. Access to the FPGA for custom processing requires -FDK option and bitfiles that have been created using either of these legacy Keysight applications:
    - U5340A FPGA Development Kit.
    - W1462BP SystemVue FPGA Architect

Hardware Platform

Hardware Overview

The M9703B is a flexible modular wideband digital receiver/digitizer offering scalable features depending on application requirements. The standard configuration implements 8 channels of 12-bit resolution with DC to 650 MHz input frequency range (-3 dB analog bandwidth), and acquiring data at 1 GS/s. If higher speed is required, the -SR2 option enables the 8 channels to sample at 1.6 GS/s. An interleave option (-INT) also allows 2 channels to be combined and reach 3.2 GS/s with -SR2 option in 4-channel acquisition mode. For higher frequency signals, the -F10 option provides an extended input frequency range of DC up to 2 GHz[1] in non-interleaved mode, or DC up to 1.4 GHz when interleaving channels[2].

Block Diagram

The M9703B implements four Xilinx Virtex-6 FPGAs dedicated to data processing. The four data processing units (DPU) implement a standard digitizer functionality firmware by default, allowing digitization of the signal, storage of the resulting data in the on-board memory and transfer through the PCIe connection to the AXIe backplane bus.
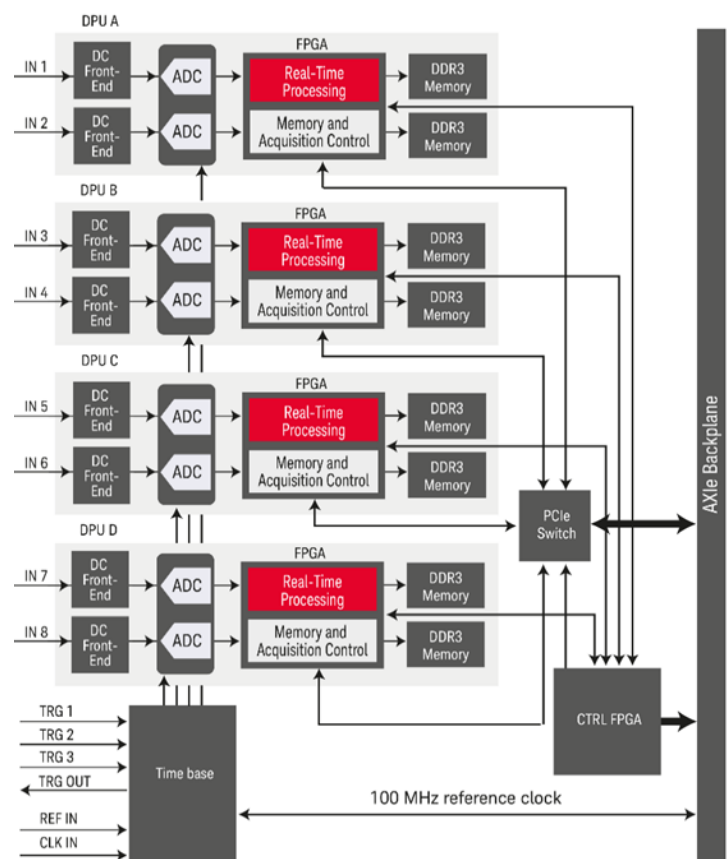

Figure 1. Simplified block diagram of the M9703B AXIe Digitizer

1. 2 GHz refers to the front-end bandwidth. The digitizer can operate in the 1st and 2nd Nyquist zones (using undersampling), but real-time bandwidth is limited by Nyquist to a maximum of [sampling rate/2], capped by the bandwidth option.
2. The fact that there is less frequency range when interleaving channels is due to internal characteristics of the ADC chipset adding filters when combining channels.

On-Board Real Time Processing

Standard digitizer functionality is further enhanced by using the FPGAs to implement real-time processing for the various firmware and application options that are available for M9703B.

The M9703B also provides access to its FPGAs for custom algorithm implementation using the -FDK option. The FPGA bitfiles for these custom algorithms can be created using either of these legacy Keysight applications[1]:

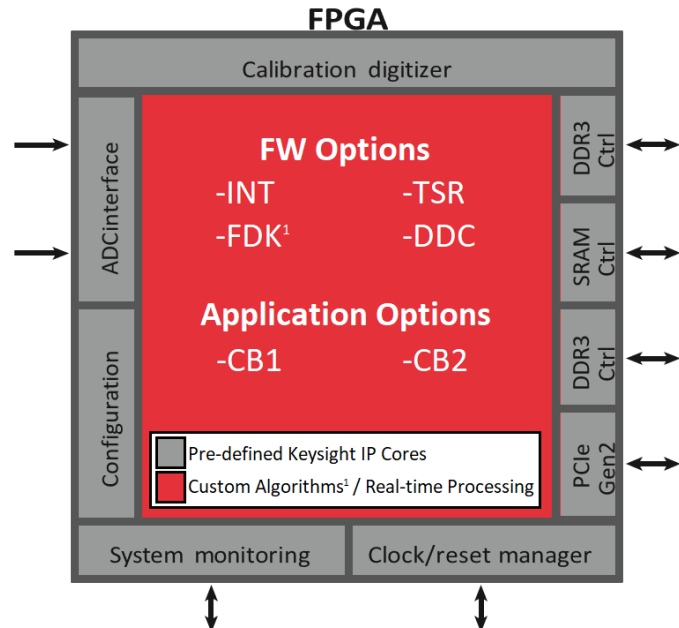- U5340A FPGA Development Kit
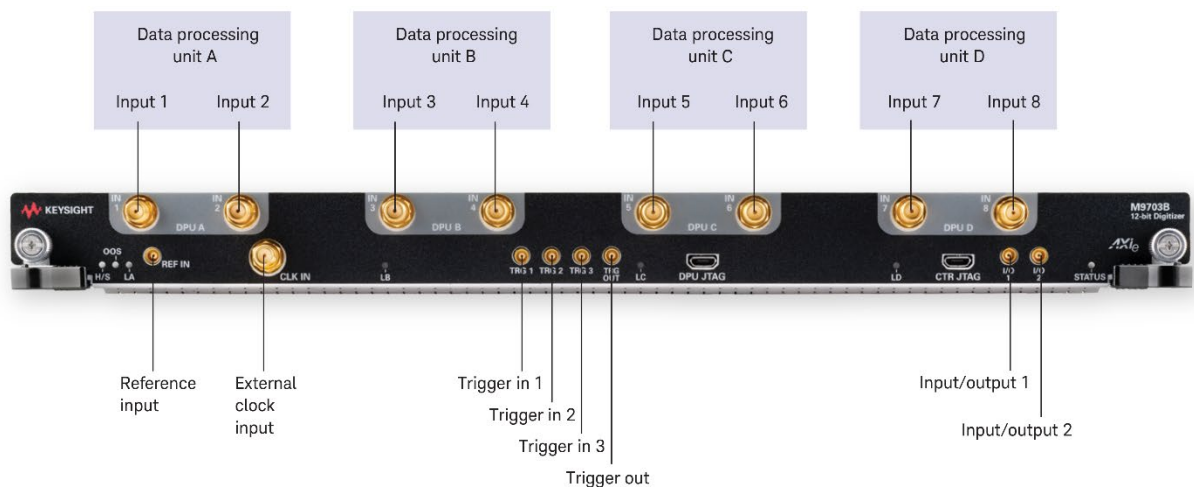- W1462BP SystemVue FPGA Architect

Figure 2. Enlarged block diagram of the FPGA

Front View

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1. The U5340A and W1462BP applications are not required to load FPGA bitfiles to M9703B; they can be loaded via the Keysight MD2 soft front panel (SFP) software application, or via an MD2 driver call.

Top View

Multichannel Data Acquisition Systems

The M9703B occupies a single slot of AXIe chassis. The architecture is modular and extensible, to provide a fully operational multichannel system in a compact format.

The examples below show some of the possible configurations:

- Two M9703B in the M9502A 2-slot chassis delivers a 16-channel 12-bit system
- Five M9703B in the M9505A or M9506A 5-slot chassis delivers a 40-channel 12-bit system
- Eight M9703B in the M9514A 14-slot chassis delivers a 64-channel 12-bit system

Figure 3. Two M9703B digitizers installed in the M9502A 2-slot chassis, forming a 16-ch 12-bit acquisition system

Figure 4. Five M9703B digitizers installed in the M9505A 5-slot chassis, forming a 40-ch 12-bit acquisition system

Secure SCPI Over LAN Functionality

The M9703B can be used with the M9506A AXIe chassis, which has been designed for demanding modular applications.

It provides 5 slots for AXIe instrument modules, up to 300 W per slot, and includes an embedded system module (ESM) that does not take up an instrument slot. The ESM provides Gen 3 x8/x16 PCIe® interfaces for connecting the chassis to an external controller or expanding the system using multiple chassis. To minimize rack space, the instrument module slots are arranged horizontally. The M9506A is the quietest AXIe chassis available with its new cooling design.

The M9506A-BC1 option adds a closed, instrument-grade, Linux-based controller to the back of the chassis. This has been developed specifically for M9703B, M9709A and M9710A digitizers to enhance security for high channel count applications, bringing the ease of use of traditional benchtop together with the benefits of a modular platform. A simple LAN connection enables easy SCPI based control of many digitizer channels in a small space[1].
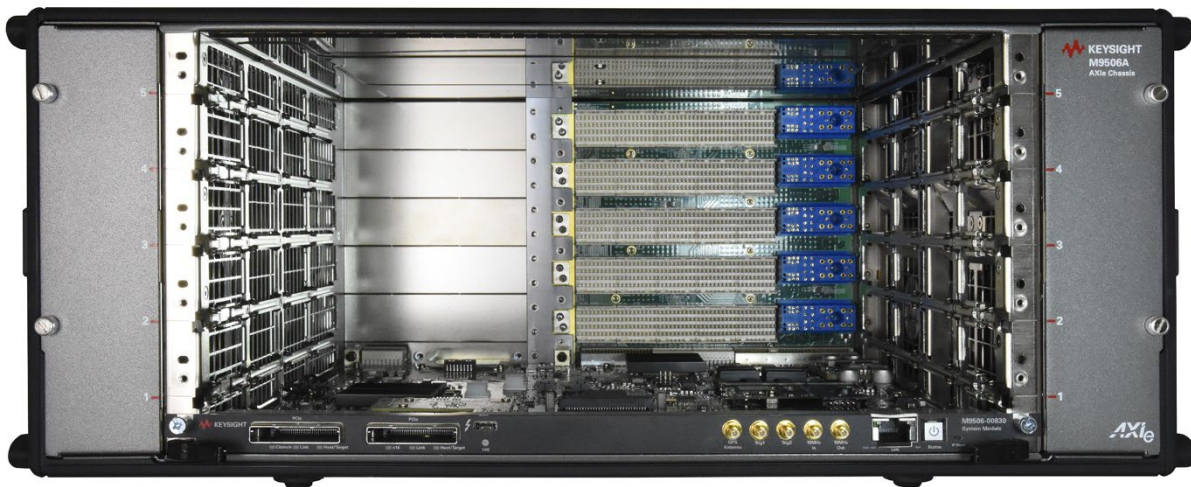

Figure 5. Keysight M9506A AXIe High-Performance 5-Slot Chassis

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1. When SCPI over LAN is enabled, PCIe communication is disabled, and the external PC controlling the digitizer does not need MD2 drivers installed.

Software Platform

I/O Libraries

Keysight IO Libraries Suite offers fast and easy access to the M9703B digitizer using a standardized interface and ensuring compatibility and upgradability of the software applications.

The Keysight IO Libraries Suite displays all the modules in your system. From here you can view information about the installed software or launch the modules' soft front panel directly from Keysight Connection Expert (KCE). In addition, KCE offers an easy way to find the correct driver for your instrument.

Drivers

The module comes with the IviDigitizer class compliant Keysight MD2 IVI-COM and IVI-C drivers that work in the most popular development environments including Visual C/C++, C#, VB.NET, MATLAB, and LabVIEW. Linux is also supported using the IVI-C driver.

Easy Software Integration

To help you get started and complete complex tasks quickly, the M9703B digitizer is supplied with a comprehensive portfolio of module drivers, documentation, examples, and software tools to help you quickly develop test systems with your software platform of choice.

Compliance

The M9703B is compliant with AXIe® and AdvancedTCA (ATCA) formats. Designed to benefit from fast data interfaces, the product can be integrated into AXIe or ATCA chassis slots. Based on ATCA, the AXIe standard implements extensions for instrumentation and test, and uses clever techniques to add powerful timing features.

Software Applications

In addition, the M9703B includes the Keysight MD2 soft front panel (SFP) graphical interface. This software application can be used to explore the capabilities of the Keysight modular high-speed digitizers.
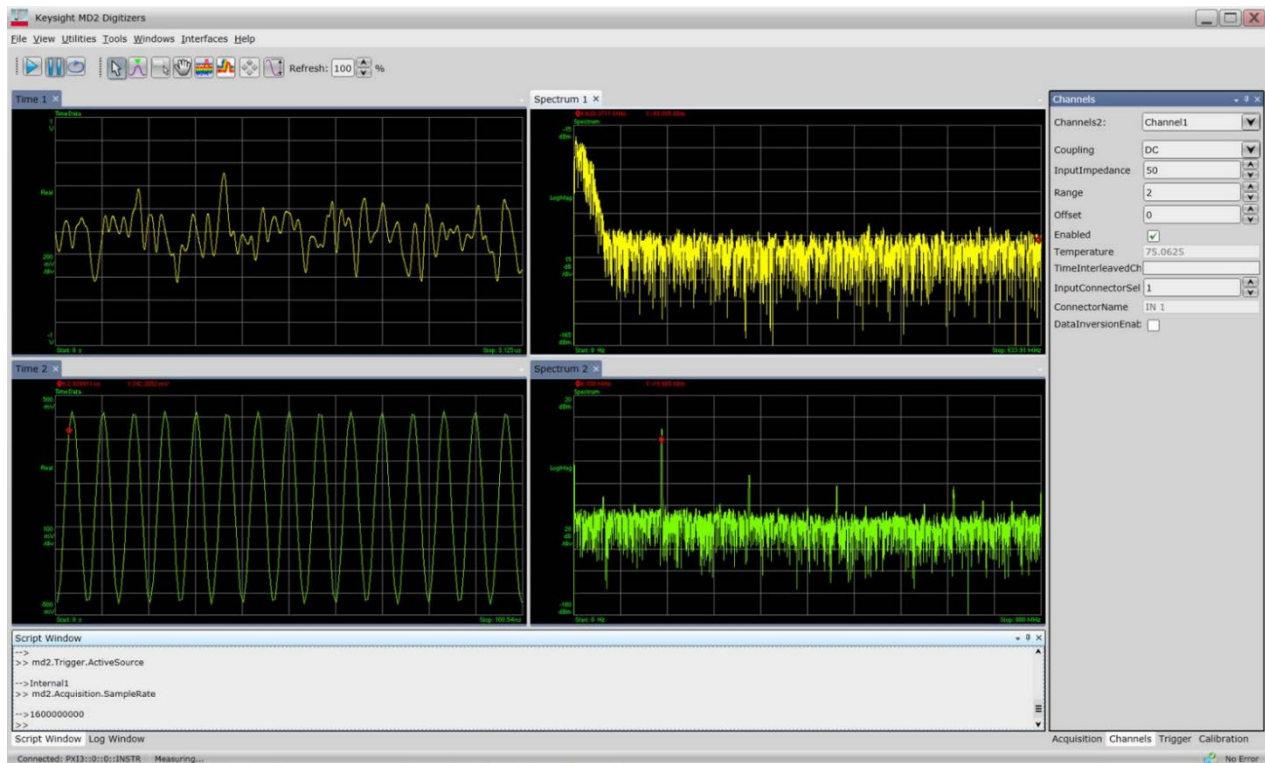

Figure 6. MD2 software front panel (SFP) interface

The M9703B is also supported by the Keysight U1092A Multichannel Acquisition Software. This provides easy control and monitoring of advanced data acquisition systems with many channels and is ideal for single-shot applications.

For advanced measurement analysis, the M9703B can be combined with Keysight's PathWave VSA Software, the industry's standard for signal analysis and demodulation. Thanks to the high data throughput of its AXIe backplane bus, the M9703B allows a much faster connection to the PathWave VSA software, compared to traditional instruments.

Firmware Options

The M9703B high-speed digitizer provides various firmware options[1]:

- DGT: Digitizer firmware
- INT: Interleaved channel sampling functionality
- FDK: Custom firmware capability
- TSR[2]: Triggered simultaneous acquisition and readout
- DDC: Wideband real-time digital down-conversion

Easy Firmware Switch

A simple call to the configuration function will switch the M9703B FPGA bitfile to the required option.
e.g. Switching the loaded firmware from the -FDK option to the -DDC option.

DGT Digitizer Firmware

This is the standard digitizer firmware which:

- Allows standard data acquisition; digitizer initialization, setting of acquisition and clocking modes, management of channel triggering for best synchronization, storing data in internal memory and/or transferring data through the backplane bus.
- Implements multi-record acquisition functionality.
- Supports fixed internal clocking frequency with internal or external reference, and variable frequency external clock.
- Offers programmable binary decimation to lower the sample rate by a factor of 2^n, where n is an integer in the range of 1 to 8 for single record mode. e.g. Decimate 1.6 GS/s to 6.25 MS/s.
- Trigger time interpolator (TTI); the high precision integrated time to digital converter can be used to increase time measurement accuracy.

INT Interleaved Channel Sampling Functionality

This option allows channels to be combined two-by-two to reach 3.2 GS/s (-SR2 option) in one channel acquisition mode.

FDK Custom Firmware Capability

This option enables the loading of custom firmware created with the legacy U5340A FPGA development kit to the four on-board Virtex-6 DPU FPGAs.

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1. Firmware option functionality cannot be mixed when running a unit with multiple options, but they can be run one after another (i.e. the -DDC function cannot be used within the -FDK option, however the customer could load an FPGA bitfile that includes their own DDC implementation as part of the custom algorithm).
2. Only available with DGT option.

TSR Triggered Simultaneous Acquisition and Readout

The TSR architecture guarantees no lost triggers at high repetition rate for specific configurations[1]:

- Larger memory size increases the maximum margin for host computer processing time and allows for short to very long record size.

- The architecture allows the continuous acquisition of new records while reading previous ones.

- High precision integrated time to digital converter can be used to increase time measurement accuracy.

DDC Real-Time Digital Down-Conversion

The real-time digital down-conversion option (-DDC), in addition to basic digitizer functionality, implements real-time digital decimation and filtering of the digitized data, allowing the user to tune and zoom on signals of interest. This exclusive IP algorithm provides very powerful and flexible digital down-conversion on both channels. The filters and local oscillators (LO) are synchronized to maintain constant phase and timing relationships allowing phase-coherent post processing.
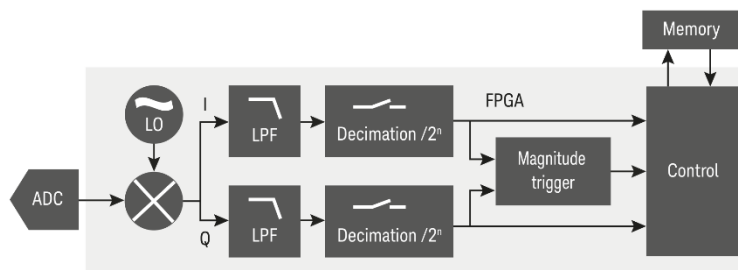

Figure 7. Single channel digital down-converter (DDC) simplified block diagram.

The -DDC option provides real-time frequency span/analysis bandwidths up to 320 MHz with -SR2 option, and up to 200 MHz with -SR1 option[2]. The center frequency of each channel can also be varied independently, ranging from DC to 1.6 GHz[3]. The -DDC option provides three main functions:

- Frequency shifting (tune)
  - Independently shifting the IF signal of each channel into baseband, allowing the analysis bandwidth to be set around the signal of interest.
- Data reduction (zoom)
  - Reducing the bandwidth and sample rate to match the analyzed signal, decreasing the amount of data that needs to be transferred for a given capture duration, which in turn accelerates post-processing operations.
- Magnitude trigger
  - Setting the magnitude level that the down converted signal needs to achieve at a specified frequency and bandwidth to generate a digital trigger on both channels.

These functions allow isolation of the signal of interest from other signals in a crowded spectrum, improving dynamic range as the integrated noise is reduced, and increasing both SNR and the effective number of bits (ENOB). The resulting advantage for your application is reduced test time, with improved overall test efficiency.

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1. Please contact Keysight to find out the repetition rate that can be achieved in your application.
2. If DDC streaming/recording is required then the -CB1 or -CB2 bundles should be considered.
3. DC to 1.6 GHz only applies if -F10 option is ordered, otherwise the upper frequency is limited to 650 MHz.

Figure 8.

The excellent channel-channel phase coherency, coupled with the wideband and flexible capability of the -DDC option, allows exceptionally fast and accurate cross-channel measurements on a large variety of signals, such as multi-tone, wideband frequency chirps, or complex signals. In this case, we show the measurement of cross-channel phase and amplitude for a 160 MHz frequency chirp.
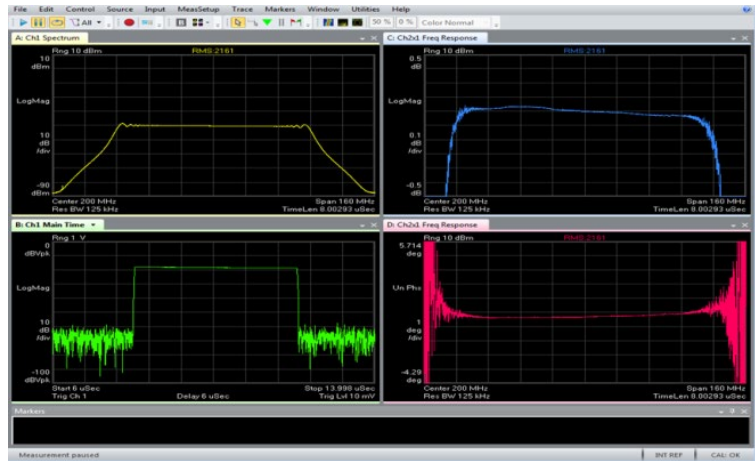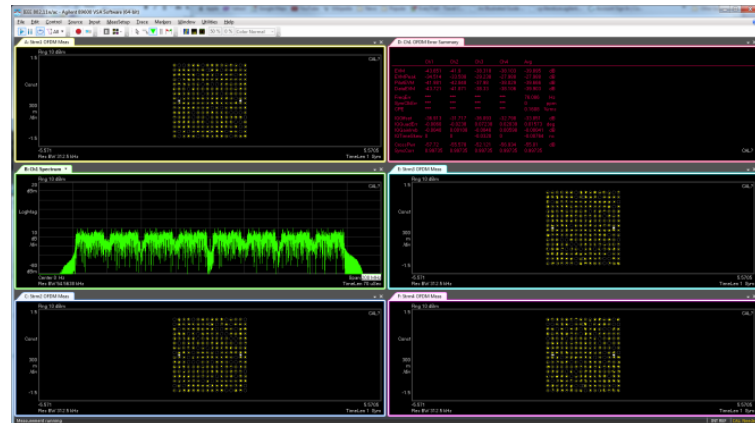

Figure 9.

The -DDC option is also ideal for emerging communications standards research and design validation. Here we show the analysis of four 802.11ac 160 MHz wide baseband signals. The M9703B allows us to reach an EVM down to -45 dB.

The wideband capability of the M9703B, combined with its excellent signal sensitivity and dynamic range, is a step toward a fully digital receiver by reducing or suppressing analog mixer stages. As an example, the M9703B wideband digital receiver/digitizer can directly digitize DVB-T signals, especially interesting for passive radar applications. When combined with the M9362AD01 quad-channel down-converter, the M9703B allows capture and analysis of wideband signals up to 50 GHz.

Figure 10.

The M9703B wideband digital receiver allows to directly digitize DVB-T signals with excellent dynamic range without the need of analog mixers, especially interesting for passive radar applications.

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Application Options

The M9703B high-speed digitizer can be configured with application specific options:

- CB1: Multichannel digital down-converter streaming and recording of I/Q data at 1 GS/s
- CB2: Multichannel digital down-converter streaming and recording of I/Q data at 1.6 GS/s

CB1/CB2 Multichannel DDC Streaming and Recording

These two bundles enable continuous gapless acquisition, implementing:

- Real time multichannel phase-coherent baseband data acquisition.
- Data streaming to host.
- Multichannel recording to disk of all I/Q samples for later analysis.

The -CB1 option is added to a pre-configured M9703B that consists of:

- 1 GS/s sampling rate (-SR1)
- Full bandwidth (-F10)
- 16 GB acquisition memory (-M16)
- Digitizer firmware (-DGT)

The -CB2 option is added to a pre-configured M9703B that consists of:

- 1.6 GS/s sampling rate (-SR2)
- Full bandwidth (-F10)
- 16 GB acquisition memory (-M16)
- Digitizer firmware (-DGT)

These streaming and recording bundles provide:

- Guaranteed recording specification[1] up to 200 MHz IBW (-CB1) or 320 MHz (-CB2), with tunable intermediate frequency.
- Data throughput optimization (I/Q samples recorded using 32-bit, 16-bit or 12-bit mode).
- Support for solutions that require multi-module synchronization (MMS) mode, allowing up to 4 modules in the same chassis to make synchronized phase-coherent recordings.
- An intuitive command line application that is used to control the digitizer.
- Support for the recording of data to PathWave VSA compatible waveform files, enabling it to be used as a graphical user interface (GUI) for the reading, display, selection, analysis, and export of data.

1. Maximum streaming and recording performance is guaranteed using an additional qualified host computer system with a specific storage configuration. Keysight can supply and install this host computer system – please contact your local Keysight office for additional information.

Technical Specifications and Characteristics

Analog Input (IN1 to IN8 SMA Connectors)

Number of channels		8 (without -INT option), 8 or 4 (with -INT option)
Impedance		50 Ω ±2 %
Coupling		DC
Full scale ranges (FSR)		1 V and 2 V (3.98 dBm and 10 dBm)
Maximum input voltage		1V FSR: Clamp at ±3.6 V, absolute max. DC voltage rating ±4.6 V 2V FSR: Clamp at ±6.3 V, absolute max. DC voltage rating ±5.0 V
Input frequency range (-3 dB bandwidth)	-F05	*DC to 650 MHz (typical)*
	-F10	*DC to 1.9 GHz (typical) in 1V FSR at 1 GS/s or 1.6 GS/s* *DC to 2.0 GHz (typical) in 2V FSR at 1 GS/s or 1.6 GS/s* *DC to 1.4 GHz (typical) at 2 GS/s or 3.2 GS/s (interleaved)*
DC gain accuracy		*±0.5% (typical)*
Offset accuracy		*±0.5% in 1V FSR* *±1.5% in 2V FSR*
Time skew[1]	Channel-to-channel skew[2]	*±50 ps (nominal) in same module* *±150 ps (nominal) between multiple modules of same chassis*
	Channel-to-channel skew stability[3]	*±200 fs pk (nominal)* *75 fs RMS (nominal)*
Phase offset	Channel-to-channel offset (@ 400 MHz)	*±7.2° (nominal) in same module* *±21.6° (nominal) between multiple modules of same chassis*
	Channel-to-channel offset stability[3]	*±0.03° pk (nominal)* *0.01° RMS (nominal)*
Input voltage offset		-2xFSR to +2xFSR
Bandwidth limit filters		*650 MHz (nominal)*
Frequency response flatness[4,5]		±1 dB from DC to 650 MHz

1. The channel-to-channel skew is defined as the magnitude of time delay difference between two digitized channel inputs, granted the same signal is provided to each channel at the exact same time.
2. The measurement represents the maximum time skew, measured with a Sinefit method on 100k samples, for a sinusoid signal at 400 MHz and averaged 10 times.
3. Skew and offset stability are measured at 25°C in a climatic chamber. The skew and offset between channels are measured every 5 minutes over 12 hours and after 1 hour stabilization time and the values represent the dispersion of the measurements. Valid for channels within a same module and across modules of a same chassis.
4. Only applicable without a bandwidth limit filter.
5. Not applicable in interleaved mode.

Analog Input (IN1 to IN8 SMA Connectors), *continued*

	@ 48 MHz	*8.7 (9.1, typical)*
	@ 100 MHz	*8.8 (9.2, typical)*
Effective number of bits (ENOB)[1]	@ 410 MHz	*8.8 (9.1, typical)*
	@ 648 MHz	*8.7 (9.0, typical)*
	@ 924 MHz	*8.3 (8.8, typical)*
	@ 48 MHz	*56 dB (58 dB, typical)*
	@ 100 MHz	*56 dB (58 dB, typical)*
Signal to noise ratio (SNR)[1]	@ 410 MHz	*55 dB (58 dB, typical)*
	@ 648 MHz	*54 dB (57 dB, typical)*
	@ 924 MHz	*52 dB (55 dB, typical)*
	@ 48 MHz	*55 dBc (60 dBc, typical)*
	@ 100 MHz	*57 dBc (62 dBc, typical)*
Spurious free dynamic range (SFDR)[1]	@ 410 MHz	*58 dBc (63 dBc, typical)*
	@ 648 MHz	*58 dBc (64 dBc, typical)*
	@ 924 MHz	*56 dBc (61 dBc, typical)*
	@ 48 MHz	*-60 dB (typical)*
	@ 100 MHz	*-62 dB (typical)*
Total harmonic distortion (THD)[1]	@ 410 MHz	*-62 dB ((typical)*
	@ 648 MHz	*-64 dB ((typical)*
	@ 924 MHz	*-61 dB (typical)*

Baseband IQ (BBIQ) Characteristics

Nominal EVM using Keysight PathWave VSA software

SISO 802.11ac 256QAM	80 MHz BW	*-45 dB (nominal) without correction filter* *-47 dB (nominal) with correction filter*
	160 MHz BW	*-43 dB (nominal) without correction filter* *-45 dB (nominal) with correction filter*
MIMO 802.11ac 256QAM, 2x2	80 MHz BW	*-45 dB(nominal) without correction filter*
	160 MHz BW	*-43 dB (nominal) without correction filter*
MIMO 802.11ac 256QAM, 4x4	80 MHz BW	*-44 dB (nominal) without correction filter*
	160 MHz BW	*-42 dB (nominal) without correction filter*
SISO LTE-A FDD DL, 2CCs full filled 64QAM	2x20 MHz BW	*-50 dB (nominal) without correction filter*
SISO LTE-A FDD DL, 4CCs Full filled 64QAM	4x20 MHz BW	*-47 dB (nominal) without correction filter*
SISO LTE-A FDD DL, 5CCs Full filled 64QAM	5x20 MHz BW	*-45 dB (nominal) without correction filter*
SISO 64 point FFT OFDM	800 MHz BW	*-42 dB (nominal) with correction filter*

1. Measured at 1.6 GS/s for a -1 dBFS input signal in internal clock mode with -F10 option.

Analog Input (IN1 to IN8 SMA Connectors), *continued*

RF characteristics		
Nominal EVM using Keysight PathWave VSA software		
GSM BTS signal	@ 900 MHz	*-51 dBc (nominal)*
	@ 1.8 GHz	*-48 dBc (nominal)*
DVB-T signal	10 MHz BW @ 850 MHz	*-53 dBc (nominal)*
Spurious-free dynamic range nominal performance measured with Keysight PathWave VSA software[1]		
SFDR	30 MHz BW @ 900 MHz	*-92 dBc (nominal)*
	80 MHz BW @ 900 MHz	*-90 dBc (nominal)*
	100 MHz BW @ 400 MHz	*-92 dBc (nominal)*
	400 MHz BW @ 400 MHz	*-87 dBc (nominal)*
	625 MHz BW @ 400 MHz	*-83 dBc (nominal)*

Digital Conversion			
Resolution			12 bits
Acquisition memory (total)		-M10	1 GB (64 M real samples/ch); standard
		-M40	4 GB (256 M real samples/ch); option
		-M16	16 GB (1 G real samples/ch); option
Sample clock sources			Internal or external
Internal clock source			Internal, external or backplane reference
	Maximum real-time sampling rates	-SR1	1 GS/s per channel; standard
		-SR2	1.6 GS/s per channel; option
		-SR1, -INT	2 GS/s; option
		-SR2, -INT	3.2 GS/s; option
	Sampling jitter[2]		*225 fs (nominal)*
	Clock accuracy		±1.5 ppm
External clock source (CLK IN SMA connector)			
	Impedance		*50 Ω (nominal)*
	Frequency range[3]	-SR1	1.8 GHz to 2 GHz; standard
		-SR2	1.8 GHz to 3.2 GHz; option
	Signal level		*+5 dBm to +15 dBm (nominal), 0 V DC*
	Coupling		AC
External reference clock (REF IN MCX connector)			
	Impedance		*50 Ω (nominal)*
	Frequency range		*100 MHz ±5 kHz (nominal)*
	Signal level		*-3 dBm to +3 dBm (nominal)*
	Coupling		AC
Acquisition modes			Single shot Sequence (multi-record)[4]

1. Measured for a CW signal of -10 dBm at the center frequency of the analyzed frequency span (BW).
2. Jitter figure based on phase noise integration from 100 Hz to 1600 MHz.
3. The sampling rate corresponds to half of the external clock frequency in 8-channel mode (non-interleaved channels). In interleaved mode (only available with the INT option), the sampling rate corresponds to the frequency of the external clock signal.
4. Up to 131,072 records. Record maximum length = memory size / number of channels.

Trigger			
Trigger modes	-DGT	Positive or negative edge	
	-DDC	Positive or negative edge, magnitude	
Trigger sources		External, Software, Channel, AXIe Synchronization	
Channel trigger frequency range		DC to 250 MHz	
External trigger (TRG 1, TRG 2, TRG 3 MCX connectors)			
	Coupling	DC	
	Impedance	*50 Ω (nominal)*	
	Level range	*±5 V (nominal)*	
	Amplitude	0.5 V pk-pk	
	Frequency range	*DC to 2 GHz (nominal)*	
Maximum time stamp duration	-SR1	52 days	
	-SR2	32 days	
Trigger time interpolator resolution	-SR1	*7.75 ps (nominal)*	
	-SR2	*6.25 ps (nominal)*	
Trigger time interpolator precision	-SR1	*20.7 ps RMS (nominal)*	
	-SR2	*15 ps RMS (nominal)*	
Rearm time	Digitizer mode	*0.8 us (nominal)*	
	DDC mode	*2.5 us (nominal)*	
Trigger out (TRG OUT MCX connector)[1]			
	Signal level	*0.8 Vpp ±2.5 Voffset (nominal)*	
Control IO (I/O A and I/O B MCX Connectors)			
Output functions		Acquisition active Trigger is armed Trigger accept resynchronization Low level High level	

Real-Time Digital Down-Conversion (-DDC Option)		
Acquisition modes		Basic digitizer or DDC digitizer[2,3]
Number of synchronous DDC channels		8 in a single module Up to 40 across 5 modules in the same M9505A chassis
Center frequency tuning range (LO)	-F10	DC to 1.6 GHz
	-F05	DC to 650 MHz
Center frequency tuning resolution		0.01 Hz
Independent channel center frequency tuning		Yes
Independent channel frequency span		No

1. At 10 MHz on a 50 Ω load.
2. Real-time DDC is active only for 1 GS/s and 1.6 GS/s sampling rate modes (non-interleaved mode).
3. In DDC mode, each sample is a pair of I & Q samples. Each sample is coded on 32 bits (16-bit I and 16-bit Q) for the highest decimated sample rate (i.e. n>0), otherwise the coding is made on 64 bits (32-bit I and 32-bit Q).

Environmental and Physical[1]		
Temperature range	Operating	0 to +45°C
	Non-operating	-40 to +70°C
EMC		Complies with European EMC Directive
		– IEC/EN 61326-1
		– CISPR Pub 11 Group 1, class A
		– AS/NZS CISPR 11
		– ICES/NMB-001
		This ISM device complies with Canadian ICES-001.
		Cet appareil ISM est conforme à la norme NMB-001 du Canada.

Power Dissipation		
-48 V		Total Power
3.4 A (nominal)		*161 W (nominal), with -DGT option*
3.6 A (nominal)		*170 W (nominal), with -DDC option*

Mechanical Characteristics		
Form factor		1 slot AXIe
Size		30 mm W x 322.2 mm H x 280 mm D
Weight		3 kg (6.61 lbs)

System Requirements		
Topic	Windows	Linux
Operating systems	Windows 10 (64-bit), all versions	Linux with Kernel versions 3.x, 4.x & 5.0 - 5.4. Linux with Kernel versions 5.15 & 6.0 are also supported but require a driver patch (available from the Linux driver page at Keysight.com)
Processor speed	1 GHz 64-bit (x64), no support for Itanium 64	As per the minimum requirements of the chosen distribution
Available memory	1 GB minimum[2]	As per the minimum requirements of the chosen distribution

Available disk space	2.5 GB available hard disk space, includes:[3]
	    – 1 GB for Keysight IO Libraries Suite
	    – 1 GB for Microsoft .NET Framework
		100 MB

Display	Minimum of 1024 x 768, 96 or 120 DPI	No display required
Browser	Use a supported version of Internet Explorer; see https://support.microsoft.com/en-gb/help/17454/lifecycle-faq-internet-explorer	Distribution supplied browser

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude, and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.
2. On older PCs with minimum RAM, installation can take a long time when installing the IO Libraries Suite and the .NET Framework.
3. Because of the installation procedure, less disk space may be required for operation than is required for installation. The amount of space listed above is required for installation. The .NET Framework Runtime Components are installed by default with most Windows installations, so you may not need this amount of available disk space.
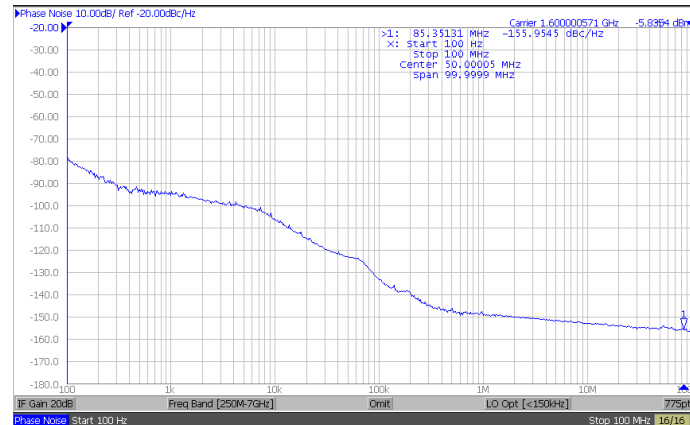
Supplemental Characteristics

Figure 11. Measured sampling clock phase noise with an internal reference clock
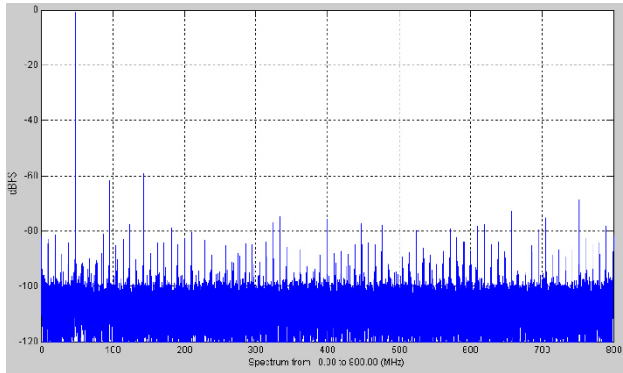

Figure 12. M9703B nominal dynamic performance in 1 V FSR for a -1 dBFS input signal at 48 MHz.
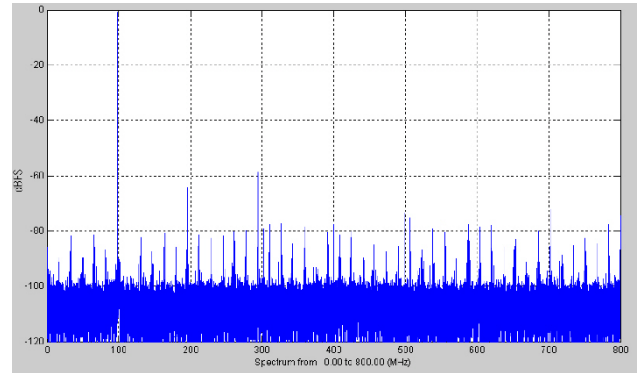

Figure 13. The FFT plot for a -1 dBFS input signal at 100 MHz in 1 V FSR shows the excellent dynamic range of the M9703B high-speed digitizer.
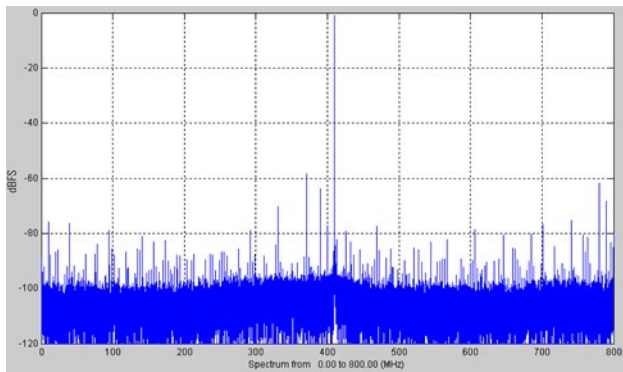

Figure 14. M9703B nominal dynamic performance in 1 V FSR for a -1 dBFS input signal at 410 MHz. Note how the dynamic range is still excellent for high frequency signals.
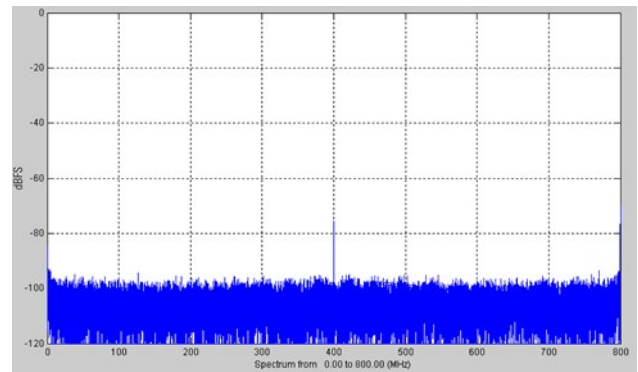

Figure 15. The M9703B nominal dynamic performance in 1 V FSR with no input signal (open input) shows a very low noise floor.
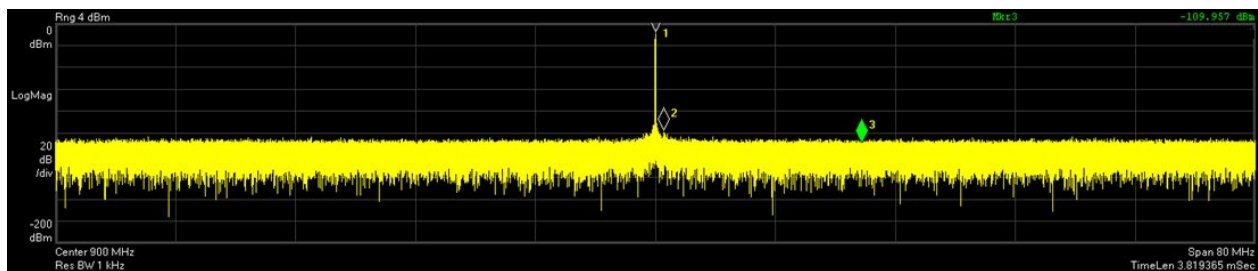
Figure 16. The exceptional noise power spectral density of the M9703B coupled with the real-time DDC allows the detection of very small signals. In this example, an 80 MHz span centered at 900 MHz, showing a very low noise floor of less than -100 dBm.
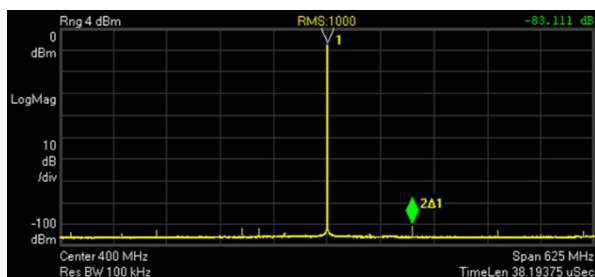

Figure 17. The M9703B has excellent dynamic range over a very wide bandwidth. In this example, the spectrum of a 400 MHz single tone signal, using the PathWave VSA software DDC, with 625 MHz frequency span centered at 400 MHz, showing -83 dBc SFDR.
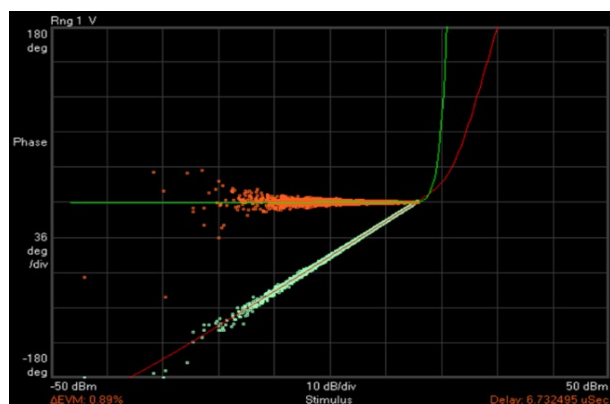

Figure 18. AM/AM and AM/PM characteristic for a 16QAM 250 MSym/s LTE signal at 400 MHz IF frequency and 400 MHz analyzed bandwidth.
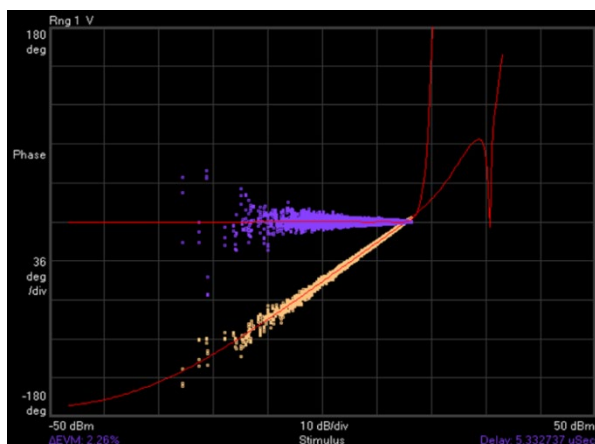

Figure 19. AM/AM and AM/PM characteristic for a 16QAM 500 MSym/s LTE signal at 400 MHz IF frequency and 625 MHz analyzed bandwidth.
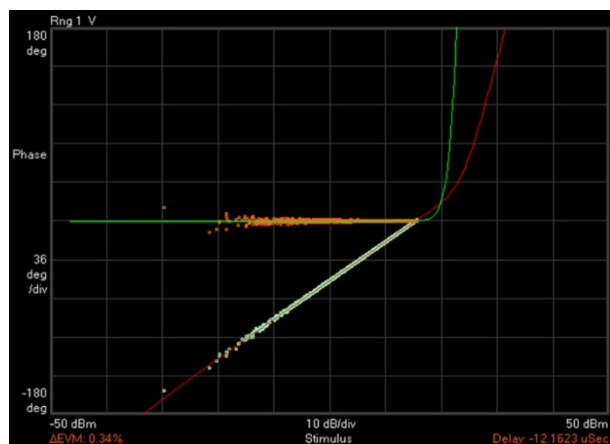

Figure 20. AM/AM and AM/PM characteristic for a 16QAM 20 MSym/s LTE signal with 400 MHz IF frequency and 100 MHz analyzed bandwidth.

Definitions for Specifications

Specifications describe the warranted performance of calibrated instruments that have been stored for a minimum of 2 hours within the operating temperature range of 0 to 45°C, unless otherwise stated, and after a 45-minute warm-up period. Data represented in this document are specifications unless otherwise noted.

Characteristics describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics are often referred to as Typical or Nominal values.

- **Typical** describes characteristic performance, which 80% of instruments will meet when operated over a 20 to 30°C temperature range. Typical performance is not warranted.
- **Nominal** describes representative performance that is useful in the application of the product when operated over a 20 to 30°C temperature range. Nominal performance is not warranted.

Note: All graphs contain measured data from several units at room temperature unless otherwise noted.

Calibration Intervals

The M9703B is factory calibrated and shipped with a certificate of calibration.

Calibration is recommended every year in order to verify product performance.

Configuration and Ordering Information

Software Information

Chassis Slot Compatibility: AXIe, ATCA

Supported operating systems	See system requirements
Keysight IO libraries	Includes: VISA libraries, Keysight Connection Expert, IO Monitor

Related Products

Model	Description
M9502A	2-slot AXIe Chassis
M9505A	5-slot AXIe Chassis
M9506A	5-slot AXIe Chassis, High-Performance
M9514A	14-slot AXIe Chassis
M9048B	PCIe Desktop Adapter, PCIe Gen 3 (x8)
Y1202A	PCIe Cable, 2.0 m Long, PCIe Gen 3 (x8)
M9537A	AXIe High Performance Embedded Controller
U1092A-S0x	Keysight MAQS Multichannel Acquisition Software
M9709A	AXIe 8-bit Digitizer, 32 Channels
M9710A	AXIe 10-bit Digitizer, 4 Channels
89601200C	Keysight PathWave VSA Software, Transportable License

Accessories

Model	Description
U5300A-104	MCX Male to SMA Male Cable, 1 m Long
U5300A-105	MCX Male to BNC Male Cable, 1 m Long
U5300A-110	XA110 SMA Input Overvoltage Protection Kit

Typical System Configuration

Model	Description
M9703B	AXIe 12-bit Digitizer, 8 Channels
M9505A	5-slot AXIe Chassis
M9048B	PCIe Desktop Adapter, PCIe Gen 3 (x8)
Y1202A	PCIe Cable, 2.0 m Long, PCIe Gen 3 (x8)

Ordering Information

Model	Description	
M9703B	AXIe High-Speed Digitizer/Wideband Digital Receiver, 12-bit, 3.2 GS/s, 8-ch, FPGA Signal Processing	
	Includes:	Software, example programs and product information on CD MCX male to BNC male cable, 1 m (qty 2)

Configurable Options

	Sampling Rate	
✓	M9703B-SR1	1 GS/s sampling rate version (2 GS/s sampling rate with -INT option)
	M9703B-SR2	1.6 GS/s sampling rate version (3.2 GS/s sampling rate with -INT option)
	Bandwidth	
✓	M9703B-F05	Input Frequency: DC to 650 MHz
	M9703B-F10	Input Frequency: DC to 2 GHz (non-interleaved) Input Frequency: DC to 1.4 GHz (interleaved)
	Memory	
✓	M9703B-M10	1 GB (64 MSample/ch) acquisition memory
	M9703B-M40	4 GB (256 MSample/ch) acquisition memory
	M9703B-M16	16 GB (1 GSample/ch) acquisition memory
	Firmware	
✓	M9703B-DGT	Digitizer firmware
	M9703B-DDC	Real-time digital down-conversion (200 MHz with -SR1, 320 MHz with -SR2)
	M9703B-INT	Interleaved channel sampling functionality
	M9703B-FDK	FPGA programming access
	M9703B-TSR	Triggered simultaneous acquisition and readout
	Applications	
	M9703B-CB1	Digital down-converter streaming at 1 GS/s
	M9703B-CB2	Digital down-converter streaming at 1.6 GS/s

Services

Calibration	
M9703B-UK6	Commercial Calibration Certificate with Test Data
M9703B-A6J	ANSI Z540-1-1994 Calibration
M9703B-1A7	Calibration + Uncertainties + Guardbanding (not Accredited)
Recalibration Service Plans	
R-50C-011-3 / 5	Calibration Plan - Return to Keysight - 3 / 5 years
R-50C-021-3 / 5	ANSI Z540-1-1994 Calibration - 3 / 5 years
Return to Service Center Warranty and Service Plans	
R-51B-001-C / 3C / 5C	Return to Keysight Warranty - 1 / 3 / 5 years
KeysightCare Service Plans	
R-55A-001-2 / 3 / 5	KeysightCare Assured - Extend to 2 / 3 / 5 years (includes Return to Keysight Extended Warranty)

✓   These options represent the standard configuration.

Instrument Upgrades

Description	Upgrade Number	Additional Information
Upgrade from M9703A to M9703B (same options)[1]	M9703BU-A2B	**Return to Keysight for upgrade**
Sampling rate upgrade from 1 GS/s to 1.6 GS/s per channel	M9703BU-SR2	**Return to Keysight for upgrade**
Bandwidth upgrade from 650 MHz to 1 GHz	M9703BU-FBW	**Return to Keysight for upgrade**
Memory upgrade from 1 GB to 4 GB	M9703BU-M40	Customer installable license key
Memory upgrade from 4 GB to 16 GB	M9703BU-M16	Customer installable license key
Memory upgrade from 1 GB to 16 GB[2]	M9703BU-M40 M9703BU-M16	Customer installable license keys
Processing upgrade from option -DGT to option -DDC	M9703BU-DDC	Customer installable license key
Upgrade to enable Interleaved sampling	M9703BU-INT	Customer installable license key
Upgrade to allow FPGA programming (custom firmware capability)	M9703BU-FDK	Customer installable license key
Triggered simultaneous acquisition and readout	M9703BU-TSR	Customer installable license key
Digital down converter streaming and recording at 1 GS/s	M9703BU-CB1	Customer installable license key
Digital down converter streaming and recording at 1.6 GS/s	M9703BU-CB2	Customer installable license key

1. The upgrade from M9703A to M9703B depends on the vintage of the instrument. Please contact your local Keysight office, providing your M9703A serial number, to confirm that it is eligible for this upgrade.
2. Upgrading from 1 GB to 16 GB requires two upgrade licenses.