User Guide

Keysight N4960A Serial BERT 17 and 32 Gb/s

KEYSIGHT TECHNOLOGIES

Notices

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Keysight Technologies, Inc.
Keysight Technologies R&D and Marketing-GmbH & Co. KG
Herrenberger Str. 130
71034 Böblingen, Germany

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Safety Notices

CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Safety Summary

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings or operating instructions in the product manuals violates safety standards of design, manufacture, and intended use of the instrument. Keysight Technologies assumes no liability for the customer's failure to comply with these requirements. Product manuals are provided with your instrument on CD-ROM and/or in printed form. Printed manuals are an option for many products. Manuals may also be available on the Web. Go to www.keysight.com and type in your product number in the Search field at the top of the page.

General

This product is a Safety Class 1 instrument (provided with a protective earth terminal). The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

All Light Emitting Diodes (LEDs) used in this product are Class 1 LEDs as per IEC 60825-1.

Environment Conditions

This instrument is intended for indoor use in an installation category II, pollution degree 2 environment. It is designed to operate at a maximum relative humidity of 15 to 85% and at altitudes of up to 2000 meters.

Refer to the specifications tables for the ac mains voltage requirements and ambient operating temperature range.

Before Applying Power

Verify that all safety precautions are taken. The power cable inlet of the instrument serves as a device to disconnect from the mains in case of hazard. The instrument must be positioned so that the operator can easily access the power cable inlet. When the instrument is rack mounted the rack must be provided with an easily accessible mains switch.

Ground the Instrument

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Do Not Operate in an Explosive Atmosphere

Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made only by qualified personnel.

Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

Safety Symbols

Table 1. Safety Symbol

Symbol	Description
	Indicates warning or caution. If you see this symbol on a product, you must refer to the manuals for specific Warning or Caution information to avoid personal injury or damage to the product.
	Frame or chassis ground terminal. Typically connects to the equipment's metal frame.
	Indicates hazardous voltages and potential for electrical shock.
	Indicates that antistatic precautions should be taken.
	Indicates hot surface. Please do not touch.
	CSA is the Canadian certification mark to demonstrate compliance with the Safety requirements.
	CE compliance marking to the EU Safety and EMC Directives. ISM GRP-1A classification according to the international EMC standard. ICES/NMB-001 compliance marking to the Canadian EMC standard.
	The RCM mark indicates that this product meets EMS/Product Safety Requirements and may be imported to Australia and New Zealand.
ICES/NMB-001	This mark indicates compliance with the Canadian EMC regulations.
ISM 1-A	This text denotes the instrument is an Industrial Scientific and Medical Group 1 Class A product.
	China RoHS regulations include requirements related to packaging, and require compliance to China standard GB18455-2001. This symbol indicates compliance with the China RoHS regulations for paper/fiberboard packaging.
	Indicates the time period during which no hazardous or toxic substance elements are expected to leak or deteriorate during normal use. Forty years is the expected useful life of the product.
	The South Korean Class A EMC declaration (KC) mark indicates that this product is Class A suitable for professional use and is for use in electromagnetic environments outside of the home. The KC mark includes the marking's identifier code that has up to 26 digits and follows this format: KCC-VWX-YYY-ZZZZZZZZZZZZZ.

Compliance and Environmental Information

Table 2. Compliance and Environmental Information

Safety Symbol	Description
	This product complies with WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste. Product Category: With reference to the equipment types in WEEE Directive Annex I, this product is classed as a “Monitoring and Control instrumentation” product. Do not dispose in domestic household waste. To return unwanted products, contact your local Keysight office for more information.

Contents

1 Setting Up the System

The N4960A serial BERT controller 17 and 32 Gb/s is shipped in a protective box. Each shipping box contains:

- N4960A-CJ0 or N4960A-CJ1 serial BERT controller.
- AC power cord.
- CD-ROM, which includes:
  - N4960A Serial BERT 17 and 32 Gb/s user guide
  - N4960A Serial BERT 17 and 32 Gb/s getting started guide
  - N4960A Serial BERT 17 and 32 Gb/s datasheet

The N4951A, N4951B, and N4952A are shipped in protective boxes with all the accessories required for operation. Each shipping box contains:

- N4951A, N4951B, or N4952A with remote head/controller cable.
- CD-ROM, which includes:
  - N4960A Serial BERT 17 and 32 Gb/s user guide
  - N4960A Serial BERT 17 and 32 Gb/s getting started guide
  - N4960A Serial BERT 17 and 32 Gb/s datasheet

1.1 Rack Mount Kit

The optional N4978A rack mount kit can be purchased separately for rack mounting the N4960A as a single unit or two instruments mounted side-by-side.

1.2 Unpacking

Carefully remove the instrument from the packaging in an ESD-safe environment.

1.3 Important Notes

- Use ESD protection at all times when using the instrument.
- Before connecting any cable to the instrument, discharge the cable by shorting the center and outer connectors of the cable together to ground momentarily.
- Review min/max specifications before applying input signals.
- Use high quality connectors on all ports. The N4951A pattern generator output and N4952A error detector input connectors are 2.92 mm, while all clock output and input connectors on the N4960A serial BERT controller are SMA. The N4951B pattern generator data output connectors are 2.4 mm.
- Leave dust jackets on unused back panel connectors.
- Situate the instrument away from heat sources, do not block the fans, and do not block the exhaust vents on the sides of the BERT controller and remote heads (minimum of 3 inches clearance).
- The bottom of a remote head can become hot to the touch. The airflow should not be blocked as this will increase the temperature.
- Power must be turned off before connecting/disconnecting a remote head.

1.4 Measurement Best Practices

- When using differential-mode connections, ensure the cables are phase balanced for best performance.
- Use high quality cables and connector savers (or adaptors).
- Keep cable lengths short and minimize the number of cable bends.
- Use an 8 in-lbs (90 N-cm) torque wrench when attaching connectors.

1.5 General Specifications

Before installing the N4960A serial BERT, review the specifications in Table 3.

Table 3. Specification considerations before installation

Parameter	Specification
Connector Type	
Controller	
All signals except 10 MHz Ref In/Out –	SMA
10 MHz In/Out	BNC
N4951A/N4952A	2.92 mm female
N4951B	2.4 mm female (data output connectors), SMA female (auxiliary connectors)
Remote Control Interface	USB2.0 and IEEE-488 (GPIB)
Operating Temperature	+15 °C to +35 °C
Storage Temperature	–40 °C to +70 °C
Line Power	
Voltage	100 to 240 VAC autoranging
Frequency	50/60 Hz
Power	170 Watts MAX
Fuse	250 V 2 A 5x20 mm (p/n 12260-002) Always replace instrument fuse with one of the same type and rating.
Dimensions (Height, Width, and Depth)	
N4960A	100 mm (3.9 in) x 214 mm (16.7 in) x 425 mm (16.7 in)
N4951A/N4952A	50 mm (1.9 in) x 109 mm (4.3 in) x 222 mm (8.7 in)
N4951B	50 mm (1.9 in) x 109 mm (4.3 in) x 273 mm (10.75 in)
Remote head/controller cable	1.0 m (39.7 in)
Weight	
N4960A	3.2 kg (7.0 lbs)
N4951A/N4952A (with cable)	0.86 kg (30.3 oz)
N4951B (with cable)	1.0 kg (35.3 oz)

Parameter	Specification
EMC	• Complies with European EMC Directive 2004/108/EC • IEC/EN 61326-1 • CISPR Pub 11 Group 1, class A • AS/NZS CISPR 11 • ICES/NMB-001 This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.
Safety	• Complies with European Low Voltage Directive 2006/95/EC • IEC/EN 61010-1, 2nd Edition • Canada: CSA C22.2 No. 61010-1 • USA: UL std no. 61010-1, 2nd Edition Acoustic noise emission Geraeuschemission LpA <70 dB LpA <70 dB Operator position Am Arbeitsplatz Normal position Normaler Betrieb Per ISO 7779 Nach DIN 45635 t.19

1.6 Safety and Regulatory

This product has been designed and tested in accordance with accepted industry standards, and has been supplied in a safe condition. The documentation contains information and warnings that must be followed by the user to ensure safe operation and to maintain the product in a safe condition.

WARNING Do not remove instrument covers. There are no user serviceable parts within. Operation of the instrument in a manner not specified by Keysight Technologies may result in personal injury or loss of life.

WARNING For continued protection against fire hazard, replace fuses, and or circuit breakers only with same type and ratings. The use of other fuses, circuit breakers or materials is prohibited.

WARNING To prevent electrical shock, disconnect instrument from mains before cleaning. Use a dry cloth or one slightly dampened with water to clean the external case parts. Do not attempt to clean internally.

CAUTION The Mains wiring and connectors shall be compatible with the connector used in the premise electrical system. Failure, to ensure adequate earth grounding by not using the correct components may cause product damage, and serious injury.

1.6.1 Declaration of Conformity

A EU declaration of conformity is available at http://regulations.corporate.Keysight.com/doc/search.htm

1.7 Installation

The following procedure describes how to install the N4960A serial BERT.

1. Install on a flat surface with unobstructed airflow to the back panel and side vents.
2. Plug the AC power cord into a suitable wall socket (100 to 240 V AC, 50/60 Hz).

WARNING If this product is not used as specified, the protection provided by the equipment could be impaired. This product must be used in a normal condition (in which all means for protections are intact) only.

3. Plug the AC power cord into the N4960A serial BERT.
4. Connect the pattern generator to the Jitter connector on the front panel.
5. Connect the error detector or a pattern generator to the Delay connector on the front panel.

CAUTION Before switching on this instrument, make sure the supply voltage is in the specified range.

CAUTION This instrument has autoranging line voltage input. Be sure the supply voltage is within the specified range.

2 Operation Overview

2.1 Introduction

The N4960A serial BERT consists of a controller, which is a stressed clock source with multi-sourced jitter capability, and support for an externally connected pattern generator and error detector to form a BERT. When used as a clock synthesizer, the range is 1 to 16 GHz. When used with a remote head attached, the range of the clock synthesizer is 2.5 to 16 GHz for the 32 Gb/s system, or 2 to 8.5 GHz for the 17 Gb/s system. The pattern generator and error detector remote heads use half rate clock architecture, giving a data rate range of 5 to 32 Gb/s for the 32 Gb/s system, or 4 to 17 Gb/s for the 17 Gb/s system.

2.2 Features

All features can be controlled through the control panel, remotely through the GPIB or USB interface using the remote commands, or through the N4980A multi-instrument BERT software.

- Controller (stressed clock synthesizer)
  - Operation from 2.5 to 16 GHz (32 Gb/s system)
  - Operation from 2 to 8.5 GHz (17 Gb/s system)
  - Two independent sinusoidal jitter injection sources (one for N4960A-CJ0)
  - True Gaussian random jitter stress (N4960A-CJ1 only)
  - Spread spectrum clock (N4960A-CJ1 only)
  - Fully programmable clock output parameters
  - Low intrinsic jitter
  - Jittered, non-jittered, and divided outputs
  - Remote control through GPIB (IEEE 488.2) or USB2.0
  - User interface along with SCPI command set for easy automation and test system integration

- N4951A-P17/N4951A-P32 programmable pattern generator
  - N4951A-P32 data rate from 5 Gb/s to 32 Gb/s
  - N4951A-P17 data rate from 4 Gb/s to 17 Gb/s
  - 1 V (p-p) output voltage (single-ended)
  - Single ended or differential AC coupled data output with integrated bias tee
  - User definable offset and termination voltage
  - Family of PRBS patterns and predefined sample patterns
  - User programmable patterns (up to 8 Mbit memory depth)

- N4951B-D17/N4951B-D32 programmable pattern generator
  - N4951B-D32 data rate from 5 Gb/s to 32 Gb/s
  - N4951B-D17 data rate from 4 Gb/s to 17 Gb/s, 1.5 V (p-p) output voltage (single-ended)
  - 5-tap de-emphasis
  - Single ended or differential AC coupled data output with integrated bias tee
  - User definable offset and termination voltage
  - Family of PRBS patterns and predefined sample patterns
  - User programmable patterns (up to 8 Mbit memory depth)

- N4951B-H17/N4951B-H32 programmable pattern generator
  - N4951B-H32 data rate from 5 Gb/s to 32 Gb/s
  - N4951B-H17 data rate from 4 Gb/s to 17 Gb/s
  - 3 V (p-p) output voltage (single-ended)
  - Single ended or differential AC coupled data output with integrated bias tee
  - User definable offset and termination voltage
  - Family of PRBS patterns and predefined sample patterns
  - User programmable patterns (up to 8 Mbit memory depth)

- N4952A-E17/N4952A-E32 programmable error detector
  - N4952A-E32 data rate from 5 Gb/s to 32 Gb/s
  - N4952A-E17 data rate from 4 Gb/s to 17 Gb/s
  - Auto sample voltage and delay alignment (can be manually set)
  - Auto detects PRBS patterns
  - Single ended or differential AC coupled data input
  - User definable termination voltage

2.3 Control

System configuration settings are all available from the local control panel interface, the remote GPIB (IEEE 488.2) interface, or the USB interface. Instrument status is conveyed on the front panel by the display.

The N4960A serial BERT is supported by the N4980A multi-instrument BERT software Version 2.2 or higher, which provides a complete user control interface and off line pattern editing and management tool.

2.4 Introduction to Stress

The N4960A serial BERT controller contains a stressed clock synthesizer. The term “Stress” refers to the ability to modulate the output signal with a calibrated level of timing jitter. Timing jitter is the short term variation of a signal with respect to its ideal position in time. Timing jitter can be seen and measured at the signal logic state transitions.

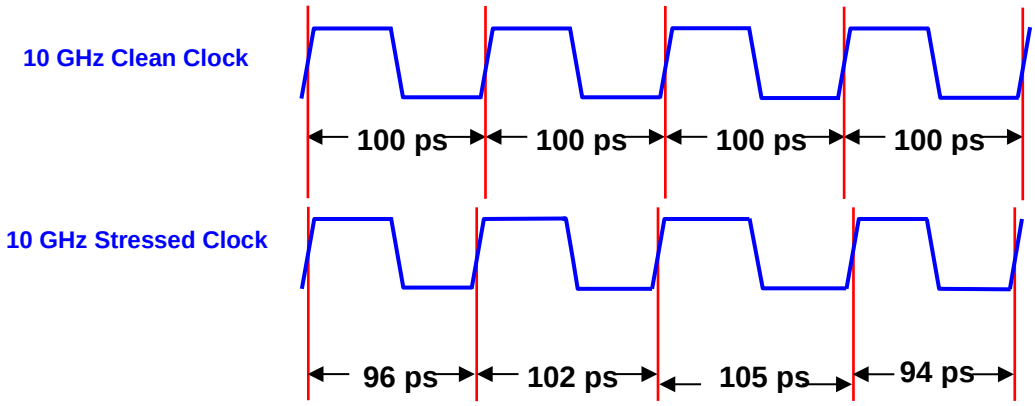


Figure 1. Timing Jitter

Amplitude jitter, also known as “interference” or simply noise, will act on the finite rise and fall times of transitions to produce effective timing jitter. The N4960A serial BERT controller does not generate interference (amplitude jitter). From this point forward, the term timing jitter will be reduced to simply jitter.

In serial data systems, excessive jitter acts to “close the eye” which will eventually result in bit errors, as the bit transition moves closer to the receiver’s decision point time window.

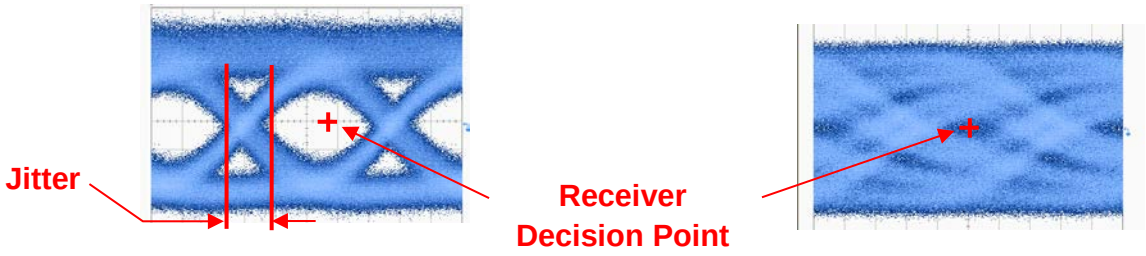


Figure 2. Eye closure with low (left) and high level of jitter (right)

A common test for a serial data receiver is its susceptibility to jitter. The test is performed by driving a known data pattern into the receiver using the N4951A/N4951B pattern generator which is stressed with a known amount of jitter. The received data is compared to an internal reference pattern of the N4952A error detector, and the number of incorrect detected bits is counted. By varying the characteristics of the jitter used to modulate the test data generator, the receiver’s performance can be characterized.

2.4.1 Quantifying Jitter

The level or “amplitude” of jitter refers to the instantaneous displacement in time of the measure point (transition) from its ideal location. When applied to a stress generator, the amplitude refers to a level of reoccurring jitter, rather than a single instantaneous edge displacement. The jitter amplitude will be stated as a peak to peak displacement, or a root means squared (rms) value, depending on the nature of the jitter distribution.

2.4.2 Types of Jitter / Stress

The jitter that a serial data receiver is exposed to in an operating environment is a composite of several elemental types. These types correspond to mechanisms in the environment which create the jitter, and are duplicated in the data pattern generator clock used to test a receiver.

The “type” of jitter represents its distribution when looking at a continuous measurement of edge displacement over time. The representation of this is a time interval error (TIE) plot. The TIE plot is a graph of the absolute displacement of each transition edge in the jittered waveform with respect to its ideal location versus time (or bit location).

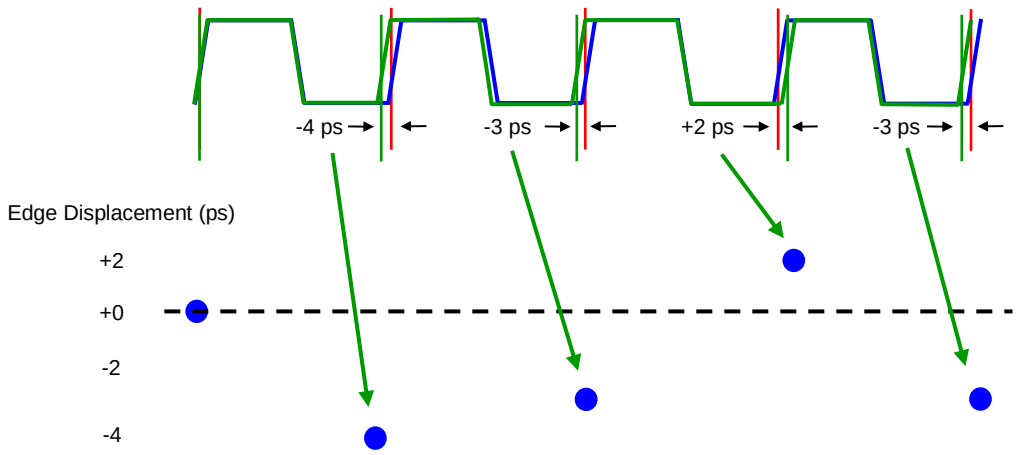


Figure 3. Time Interval Error plot of edge displacement

The resulting TIE plot shows the modulation of the jitter. The wave shape of the modulation envelope (TIE plot), relates to the type of jitter in the signal.

Jitter can be qualified as being one of a combination of several types, which again refer to the wave shape of the deviation versus time. The most basic distinction is deterministic versus non-deterministic. As its name implies, deterministic jitter forms a pattern which can be recognized. Deterministic jitter can be further broken down into data dependent, which is synchronous to the data pattern, and periodic, which has frequency components that are asynchronous to the data. While periodic jitter can have any wave shape, sinusoidal (SJ) is the most common.

The jitter amplitude (deviation in time from ideal location) of deterministic jitter is bounded. Once enough transition edges have been sampled to determine the peaks of the TIE envelope, additional sampling will not show an increase in the peak instantaneous jitter. A common graphical representation of jitter is referred to as a TIE histogram, or simply a jitter histogram. The histogram shows peak deviation versus number of samples. Figure 4 shows a typical TIE histogram plot of sinusoidal jitter.

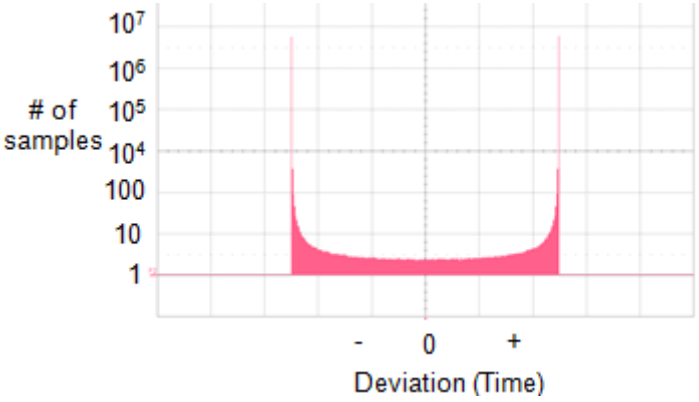


Figure 4. TIE histogram of pure sinusoidal jitter

The horizontal axis is jitter magnitude—deviation in time of the actual edge location relative to its ideal location. The axis has polarity, with 0 deviation occurring in the center. Points to the right of center are from transitions which occur after the ideal location (lag), while those to the left of center occur before the ideal location (lead).

The vertical axis shows the number of occurrences, plotted on a log scale. The characteristic shape reflects what is expected from a sine wave. The amplitude is near the positive and negative peak for most of the time, and in the zero crossing point for the least amount of time.

Generating a jitter histogram of pure deterministic jitter with a measurement instrument which updates the plot as additional samples are taken would quickly fill out the envelope, with no change in shape or peaks as additional samples are taken.

Because deterministic jitter is bounded, its magnitude is usually expressed as a peak to peak value. The units are either absolute time, for example picoseconds (ps), or relative to bit time, in unit intervals (UI).

Non-deterministic jitter is composed primarily of random jitter components. As the name implies, the envelope of random jitter will have no recognizable pattern. Random jitter results from noise artifacts in the system. Non-deterministic jitter is un-bounded. As more samples are measured, the TIE histogram will show ever increasing peak jitter, occurring at small number of samples, with the process unending. The TIE histogram of pure random jitter (RJ) will have a true Gaussian deviation, as shown in Figure 5.

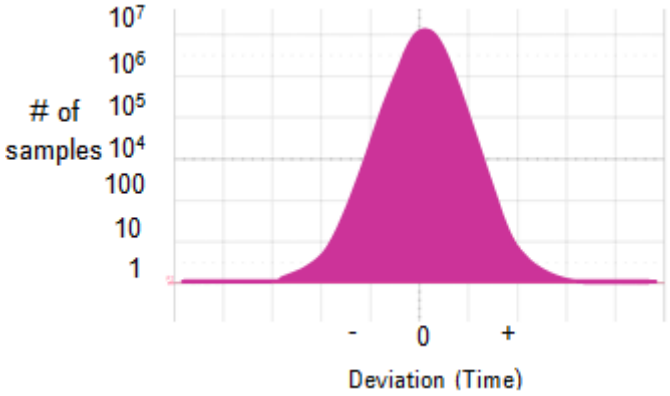


Figure 5. Typical TIE Histogram of Random Jitter

When only random jitter is present in the signal, the majority of transitions will occur at the ideal location in time (zero deviation), with decreasing numbers of transitions occurring at increasing levels of deviation in time. Due to the distribution, the magnitude of random jitter is usually expressed as a root mean squared (rms) value. The RJ magnitude can also be expressed as a peak to peak value, at a given confidence level. The confidence level can be computed from the number of samples. As with deterministic jitter, the units are either absolute time, for example ps, or relative to bit time, in UI.

Data and clock signals in real life operating systems will usually contain jitter which has both deterministic and non-deterministic components within it.

2.4.3 Stress for Jitter Tolerance Testing

Stressed clock synthesizers such as the N4960A serial BERT controller are used to clock a data pattern generator, which in turn is used to test a serial data receiver's susceptibility to jitter. The jitter tolerance test is the basic method generally used to characterize a receiver. The test is performed with a BERT, used to monitor the receiver detected output and determine when it does and when it does not operate error free. The test is started by operating the receiver and initializing the test setup to achieve error free operation. Then stress is added, usually as a single tone of SJ at a specific frequency with low amplitude. The SJ amplitude is increased until bit errors start to occur. The stress amplitude at this point is recorded, the SJ amplitude reduced and the frequency changed. The process then repeats at the new SJ frequency. The resulting jitter tolerance plot shows the limits of error free operation as jitter amplitude versus jitter frequency.

Some communication standards include a base line mixture of RJ and SJ to be constant throughout the test, with the larger SJ used for the measurement summed into the baseline. The addition of the baseline represents the intended operating environment.

3 Operation

3.1 General Information

The N4960A serial BERT should be used in accordance with the following:

- Read and follow operating instructions of all system equipment and do not exceed min/max specifications.
- Use ESD protection at all times, but especially when handling RF inputs/outputs.
- Before connecting any cable to the instrument, discharge the cable by shorting the center and outer connectors of the cable together to ground momentarily.
- Situate the instrument away from heat sources.
- Do not block airflow to the fans or exhaust vents and do not allow foreign material into enclosure.
- Do not modify the power plug or wall outlet to remove the third (ground) pin.
- Do not drop or shake the instrument, minimize vibration, and handle with care.
- Power must be turned off before connecting/disconnecting a remote head.

NOTE There are no user-serviceable parts within. Return damaged instruments for factory-authorized repair. Refer to instrument warranty for more information.

3.1.1 Performance Recommendations

The following recommendations ensure best performance:

- When using differential mode connection for outputs, ensure the cables are phase balanced. If the electrical length of one cable is a significant fraction of a unit interval longer than the other, the quality of the differential signal will be degraded.
- Keep cable lengths short and minimize number of cable bends.

It is not usually necessary to terminate unused outputs of a differential pair when a single ended signal is used. However, when the N4952A error detector is driven with a single ended signal, it is good practice to terminate the unused input to avoid errors from external noise.

3.1.2 Connector Care

The N4960A serial BERT controller features high-quality SMA connectors for the front and rear panel input and output connections while the N4951A pattern generator and N4952A error detector use 2.92 mm. The N4951B pattern generators use type 2.4 mm connectors for data output and SMA for auxiliary input/output connectors. Connector damage will degrade signal fidelity.

Use high quality SMA-connectors on the SMA ports. Always leave dust jackets on unused ports. Tighten the connectors to 8 in-lbs (90 N-cm) to assure proper mating.

Refer to the N4960-90030 N495xA through N498xA Connector Care Reference Guide at www.Keysight.com/find/N4951A.

Inspect the connectors for the following:

- Worn or damaged threads
- Scratches to mating surface
- Burrs and loose metal particles
- Dust or foreign material in the space surrounding the center pin
- Ensure that female contacts are straight and aligned

Clean the connectors as described in the following procedure. Cleaning connectors with alcohol shall only be done with the instruments power cord removed, and in a well-ventilated area. Allow all residual alcohol moisture to evaporate, and the fumes to dissipate prior to energizing the instrument.

1. Remove any dust or loose particles using a low-pressure air source.
2. Moisten a lint-free swab with isopropyl alcohol. Do not saturate the swab.
3. Minimize the wicking of the alcohol into the connector structure.
4. Clean the mating plane surfaces and threads.
5. Allow alcohol to evaporate, and then use a low-pressure air source to blow surfaces clean.
6. Make sure no particles or residue remains.
7. Inspect connector for damage.

3.2 Power on Settings

On power on, the instrument always returns to the factory preset settings, listed in 8 Appendix A Preset State. Users who wish to quickly return to last used settings may save them in one of the 5 saved settings locations, and recall them on power on.

3.3 N4960A Serial BERT Controller Front Panel

The N4960A serial BERT controller front panel indicates the system status and contains the control panel for local operation of the instrument.

Figure 6 shows the front panel of the N4960A serial BERT controller.

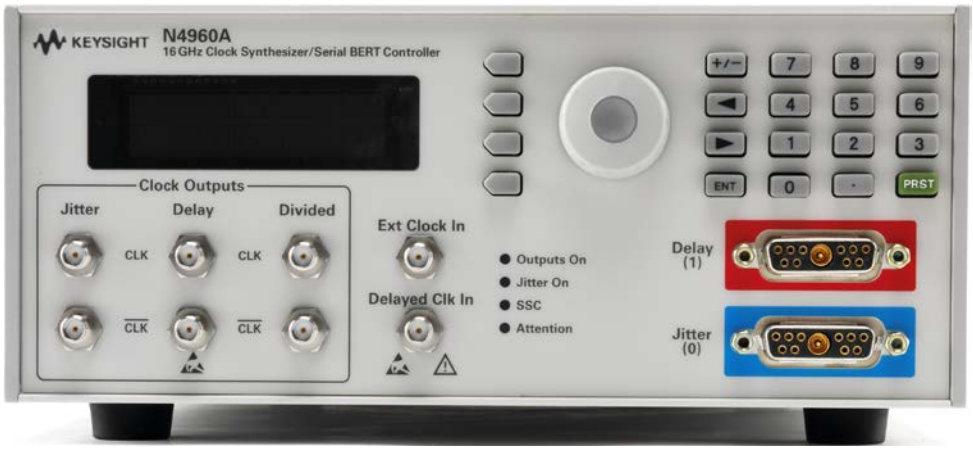


Figure 6. N4960A serial BERT controller front panel

Table 4 describes the N4960A serial BERT controller front panel functions.

Table 4. N4960A serial BERT controller front panel

Item	Description
Display	The display is part of the control panel and is used to view the menu structure.
Softkey buttons	The four softkey buttons to the right of the display are part of the control panel and are used to switch between menu items, move the highlight up or down, and edit or select parameters.
Rotary knob	The rotary knob is part of the control panel and is used to increase or decrease a numeric value and move the highlight to the next digit, character, or item in a list.
Keypad	The keypad is part of the control panel and is used to enter numeric values for parameters. The PRST hardkey button is used to perform an instrument preset.

Item	Description
Clock outputs	
Jitter	The jitter output is the main stressed clock output. The clock phase can be modulated in time with one or more calibrated jitter sources. The output amplitude, offset, and termination voltage are also user settable. The jitter sources are: • Sinusoidal jitter 1 (SJ1) • Sinusoidal jitter 2 (SJ2) (N4960A-CJ1 only) • Sinusoidal periodic jitter (PJ) • Externally supplied jitter • Random jitter (RJ) is internally sourced (N4960A-CJ1 only) Sinusoidal jitter 1, Sinusoidal jitter 2, random jitter, and external jitter (high frequency band) can be enabled simultaneously. However, the sum of these paths must be kept below the specified maximum modulation level. In addition, the periodic jitter path or external low band (high deviation) jitter path cannot be enabled if any of the other jitter paths are enabled. By disabling the stress sources, this output can be used to provide a clean (non-jittered) clock. The jitter output also provides the clock source for the pattern generator. When used as a BERT, the synthesizer clock frequency is set to 1/2 of the BERT data rate. Any stress applied to the jitter clock output will appear on the pattern generator output (channel 0 only) at 2x the amplitude of the clock jitter.
Delay	The delay differential output provides a non-stressed clock output with adjustable phase offset (in UI) as well as amplitude, offset, and termination voltage adjustment. The delay clock is also used to clock the error detector. When operating as a BERT, both auto and manual detector alignment will alter the delay setting for the front panel output. Conversely, manually setting the delay output delay value may degrade the error detector operation by misaligning the detector sample point. The value of delay applied to the delay clock output will appear on the error detector or pattern generator output (channel 1 only) at 2x the value of the clock delay.
Divided	The divided differential clock output produces a non-stressed signal that is related to the clock frequency by a divider factor. The divided clock output signal also has amplitude, offset, and termination voltage adjustment. By setting the divide ratio to 1, this output can be used as a non-divided clean (non-jittered) clock.

Item	Description
Ext Clock In	Accepts an external clock to be substituted for the internal synthesizer across the entire supported frequency range. When used to source the clock for the pattern generator or error detector, this input is a half-rate clock. Note: The instrument calibration requires knowledge of the clock frequency. To facilitate externally sourced clock input, it contains a frequency counter with sufficient resolution and accuracy to support this calibration. The counter and instrument systems require a finite time to respond to large frequency changes. Thus, in order to maintain calibration, the external clock must be either a stable CW (Continuous Wave) signal, or modulated over relatively low frequency (< 100 MHz) at low rates of change.
Delayed Clk In	Accepts an external signal which can be used to clock the error detector. This would commonly be sourced from an external clock recovery unit. When used with the error detector, this input is a half-rate clock (one half the error detector data rate). Note: The instrument calibration requires knowledge of the applied clock frequency. Unlike the external clock input, the instrument does not have an internal counter to determine the delay clock frequency, and so the frequency should be entered by the user. If no value is entered, the instrument defaults to the main clock frequency.
Status LEDs	
Outputs On	The Outputs On LED indicator is lit when any of the clock outputs are turned on.
Jitter On	The Jitter On LED indicator is lit when any stress source is enabled.
SSC	The SSC LED indicator is lit when the spread spectrum clock function is enabled.
Attention	The Attention LED indicator is lit when an error has occurred. The indicator will not turn off until the error message has been cleared in the Error Log in the System menu.

Item	Description
Delay	An error detector or pattern generator can be connected to the Delay connector (channel 1). The clock signal for the error detector or pattern generator is derived from the Delay clock output.
Jitter	A pattern generator can be connected to the Jitter connector (channel 0). The clock signal for the pattern generator is derived from the Jitter clock output.

3.4 N4960A Serial BERT Controller Rear Panel

Figure 7 shows the N4960A serial BERT controller rear panel.

Figure 7. N4960A serial BERT controller rear panel

Table 5 describes the N4960A serial BERT controller rear panel functions.

Table 5. N4960A serial BERT controller rear panel

Item	Description
USB Connector	The USB connector is a type B USB port that connects the N4960A serial BERT controller to an external PC for remote operation.
GPIB Connector	The GPIB connector is a general purpose interface bus (GPIB, IEEE 488.1) connection that can be used for remote operation.
Ext Jit In	Accepts an external jitter source for either the low or high frequency band modulation paths. Low band input must be sinusoidal wave shape, with frequency in the range of 1 Hz to 4 MHz.
RJ Out and RJ In Connectors	The RJ loop through path is used for inserting modulation frequency contour filters in the random jitter path. The signal impedance is 50 Ω.

Item	Description
10 MHz In Connector	The 10 MHz In connector accepts a 10 MHz reference signal from an external source to allow the synthesizer to be phase locked to an external reference clock.
10 MHz Out Connector	The 10 MHz Out connector is a 10 MHz reference output used to lock the frequency reference of other equipment to the N4960 serial BERT controller.
Label	N4960A serial BERT controller serial number.
Fuse Drawer	Contains the primary power mains fuse. To replace, remove the fuse by depressing the snap in tab and withdrawing the fuse drawer. A blown primary fuse generally indicates a significant component failure. The instrument should be returned to Keysight Technologies for service in the event the fuse blows.
Power Switch	N4960A serial BERT controller main power switch (1=On; 0=Off).
Power Input Connector	Connect to power mains using approved power cable.

3.5 N4951A Front Panel

Figure 8. N4951A front panel

Table 6. N4951A front panel

Item	Description
Ch ID LED	The Channel ID LED indicator is lit when connected to the N4960A serial BERT controller.
Atten LED	The Attention LED indicator is lit when an error has occurred. The indicator will not turn off until the error message has been cleared in the Error Log in the System menu.
On LED	
Output Off	The On LED indicator is off when the data output is turned off.
Output On	The On LED indicator is lit when the data output is turned on.
Data Output	The differential data outputs are 2.92 mm connectors.

Item	Description
Connectors	
Aux In	This connector is reserved for future enhancements.
Aux Out	The Auxiliary Output 2.92 mm connector provides a pattern trigger.

3.6 N4951A Rear Panel

Figure 9. N4951A rear panel

Table 7. N4951A rear panel

Item	Description
Controller Connector	The D-subminiature connector receives clock signals, control signals, and power supplies from the controller via the 1 meter remote head/controller cable.
Label	Shows the N4951A option number (-P17 or -P32) and serial number.

3.7 N4951B-D17/-D32 Front Panel

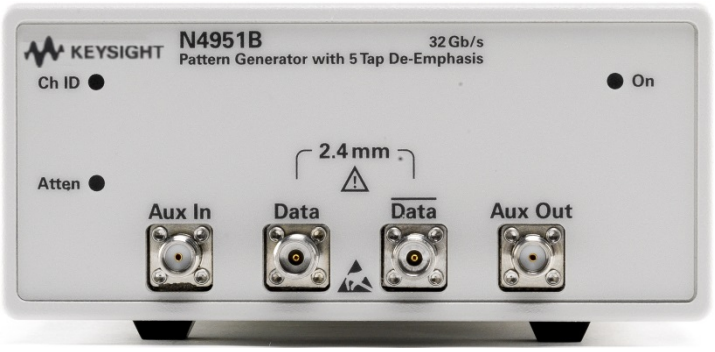


Figure 10. N4951B-D17/-D32 front panel

Table 8. N4951B-D17/-D32 front panel

Item	Description
Ch ID LED	The Channel ID LED indicator is lit when connected to the N4960A serial BERT controller.
Atten LED	The Attention LED indicator is lit when an error has occurred. The indicator will not turn off until the error message has been cleared in the Error Log in the System menu.
On LED	
Output Off	The On LED indicator is off when the data output is turned off.
Output On	The On LED indicator is lit when the data output is turned on.
Data Output Connectors	The differential data outputs are 2.4 mm connectors.
Aux In	This connector is reserved for future enhancements.
Aux Out	The Auxiliary Output SMA connector provides a pattern trigger.

3.8 N4951B-D17/-D32 Rear Panel

Figure 11. N4951B-D17/-D32 rear panel

Table 9. N4951B-D17/-D32 rear panel

Item	Description
Controller Connector	The D-subminiature connector receives clock signals, control signals, and power supplies from the controller via the 1 meter remote head/controller cable.
Label	Shows the N4951B option number (-D17 or -D32) and serial number.

3.9 N4951B-H17/-H32 Front Panel

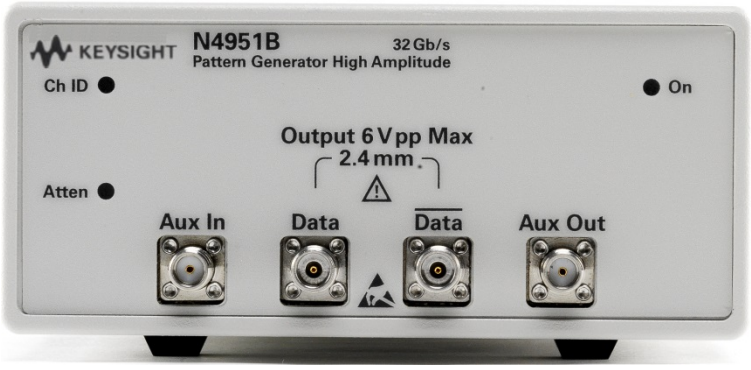


Figure 12. N4951B-H17/-H32 front panel

Table 10. N4951B-H17/-H32 front panel

Item	Description
Ch ID LED	The Channel ID LED indicator is lit when connected to the N4960A serial BERT controller.
Atten LED	The Attention LED indicator is lit when an error has occurred. The indicator will not turn off until the error message has been cleared in the Error Log in the System menu.
On LED	
Output Off	The On LED indicator is off when the data output is turned off.
Output On	The On LED indicator is lit when the data output is turned on.
Data Output Connectors	The differential data outputs are 2.4 mm connectors.
Aux In	This connector is reserved for future enhancements.
Aux Out	The Auxiliary Output SMA connector provides a pattern trigger.

3.10 N4951B-H17/-H32 Rear Panel

Figure 13. N4951B-H17/-H32 rear panel

Table 11. N4951B-H17/-H32 rear panel

Item	Description
Controller Connector	The D-subminiature connector receives clock signals, control signals, and power supplies from the controller via the 1 meter remote head/controller cable.
Label	Shows the N4951B option number (-H17 or -H32) and serial number.

3.11 N4952A Front Panel

Figure 14. N4952A front panel

Table 12. N4952A front panel

Item	Description
Ch ID LED	The Channel ID LED indicator is lit when connected to the controller.
Atten LED	The Attention LED indicator is lit when an error has occurred. The indicator will not turn off until the error message has been cleared in the Error Log in the System menu.
Run LED	BLUE while an accumulated BER measurement is running.
Errors LED	OFF when no errors are detected, RED when errors are detected.
Data Loss LED	RED when data is not detected.
Sync Loss LED	RED when data is detected but the data pattern cannot be synchronized.
Data Input Connectors	The differential data inputs are 2.92 mm connectors.
Aux In	This connector is reserved for future enhancements.
Aux Out	The Auxiliary Output connector provides an error trigger.

3.12 N4952A Rear Panel

Figure 15. N4952A rear panel

Table 13. N4952A rear panel

Item	Description
Controller Connector	The D-subminiature connector receives clock signals, control signals, and power supplies from the controller via the 1 meter remote head/controller cable.
Label	Shows the N4952A option number (-E17 or -E32) and serial number.

3.13 Block Diagram (32 Gb/s system)

Figure 16 is a simplified block diagram of the 32 Gb/s system that emphasizes all inputs and outputs.

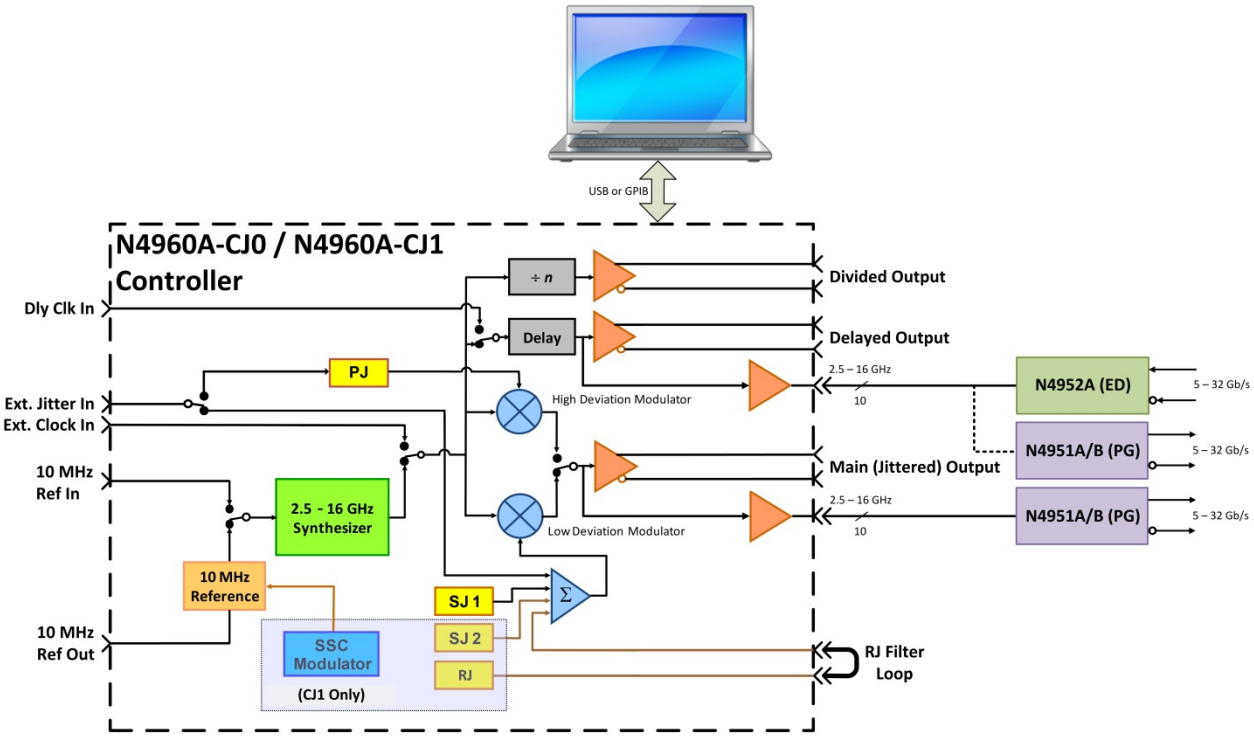


Figure 16. Simplified block diagram (32 Gb/s system)

3.14 Block Diagram (17 Gb/s system)

Figure 17 is a simplified block diagram of the 17 Gb/s system that emphasizes all inputs and outputs.

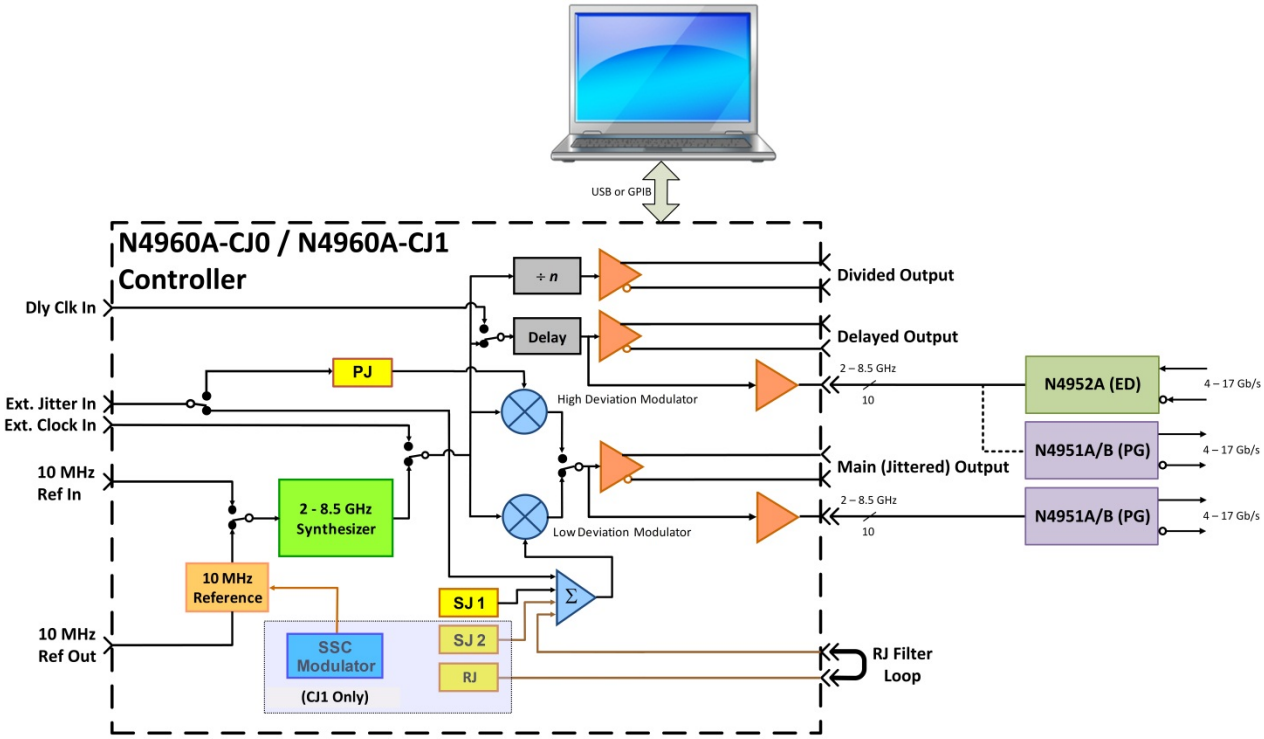


Figure 17. Simplified block diagram (17 Gb/s system)

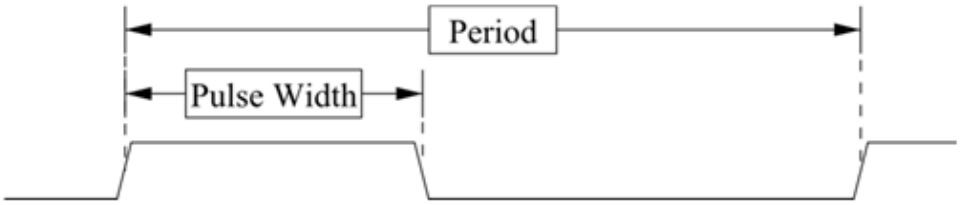
3.15 N4960A Serial BERT Controller

3.15.1 Divided Clock Output

The N4960A serial BERT controller has the capability to divide the clock frequency over a broad range of divide ratios and return the divided signal as fully differential non-stressed outputs with adjustable amplitude and offset. This provides the user a convenient method for generating a trigger signal to use with a scope, or other applications requiring a sub rate clock.

The divide ratios are 1 to 99,999,999 with no missing integers. The divided clock settings can be controlled programmatically or through the front panel.

The divided clock output duty cycle varies between 33% and 66% as a function of the divide ratio, N. When N is a power of two, the duty cycle is exactly 50%. As N deviates from a power of two, the duty cycle deviates from 50%. For example, N=64 has 50% duty cycle, N=60 has 47% duty cycle, and N=56 has 43% duty cycle. Figure 18 shows the formulas for calculating pulse width and duty cycle as a function of N, for any integer N from 2 to 99,999,999. The duty cycle of the divided clock is 50% ± 10% when the divide ratio is set to 1.



$$Pulse\ Width\ (input\ cycles) = N - 2^{floor\left[\frac{log10(\frac{N}{3})}{log10(2)}+1\right]}$$

$$Duty\ Cycle\ (\%) = (Pulse\ Width / N) * 100$$

Figure 18. Calculating pulse width and duty cycle

Figure 19 is a plot of the duty cycle versus the divide ratio for N = 2 to 1024.

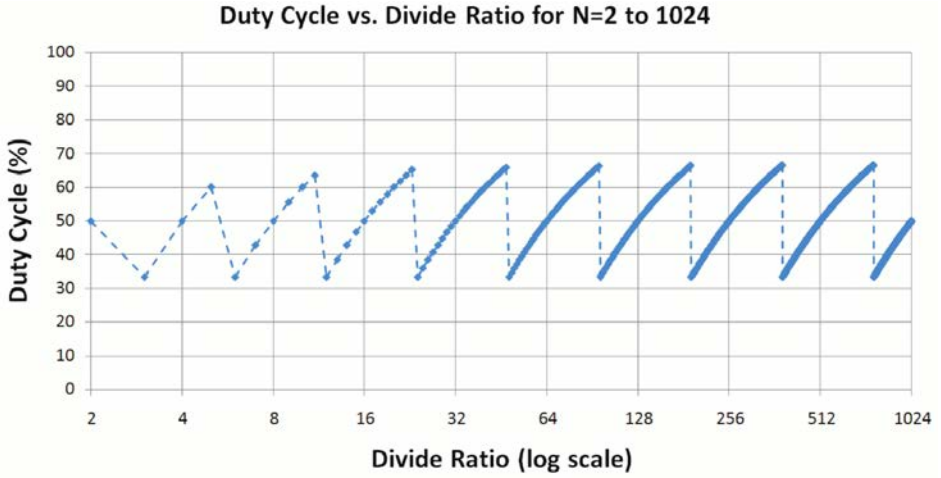


Figure 19. Duty cycle versus divide ratio

3.15.2 Delayed Clock Output

The Delayed Clock output is a non-stressed clean output with adjustable phase that can be set from -1000 UI to 1000 UI in 0.001 UI increments. When used as a clock source for a BERT, the Delayed Clock would generally be used to clock the error detector.

The Delayed Clock settings can be controlled programmatically or through the front panel.

3.15.3 Jittered Clock Output

The Jittered Clock output is the main stressed output signal. When used with a BERT, it would normally provide the clock for the pattern generator connected to the Jitter connector on the front panel of the N4960A.

The Jittered Clock output parameters can be controlled programmatically or through the front panel.

Refer to section 2.4 Introduction to Stress, for a full description of the stress implementation in the N4960A serial BERT controller.

The total stress appearing in the output is a summation of the individual active stress components available in the instrument model.

For the N4960-CJ0, the stress can be either high frequency band sinusoidal jitter (SJ1) plus externally applied high band jitter, or low frequency periodic jitter (PJ), or low frequency (high deviation) externally applied jitter.

For the N4960-CJ1, the stress source choices are one or two tones of high frequency sinusoidal (SJ1 + SJ2), summed with Random Jitter (RJ) and any externally applied high band jitter, or low frequency periodic jitter (PJ), or low frequency (high deviation) externally applied jitter.

3.15.4 Sinusoidal, Random, and External High Band Paths

The SJ1, SJ2, random jitter, and the external high frequency band (low deviation) jitter input paths can be enabled simultaneously. However, the sum of these paths must be kept below the specified maximum modulation level.

NOTE

Enabling periodic jitter or external low band jitter enables the low frequency band path (the low frequency band is the default path). Enabling SJ1, SJ2, random jitter, or external high frequency band enables the high frequency band path. Switching between low frequency band and high frequency band jitter sources or between jitter sources within the same band may cause a phase shift in the jittered clock and the pattern generator. Before performing measurements, enable the jitter source to be used for the measurement, set the amplitude to 0 UI then perform an auto alignment.

NOTE Applying an external jitter signal with amplitude which exceeds the specified maximum phase deviation from itself or as a sum with SJ1, SJ2, and/or RJ may overdrive the high frequency band modulator. Overdriving the modulator may result in distorted or intermittent clock output (clock slips). The N4960A cannot detect conditions which overdrive the modulator.

The RJ source provides true Gaussian random jitter with a crest factor of at least 14. The unfiltered spectral content is flat from DC to the contour of the high frequency band modulator, which has a -3 dB bandwidth (BW) at approximately 320 MHz. For applications which require a specified RJ frequency contour, an external filter can be placed in the RJ modulation signal path. Both a low pass and a high pass filter can be used in series when both ends of the spectrum require filtering. The RJ signal is available on the rear panel (N4960A-CJ1 only) between the RJ Out and RJ In connectors. The impedance of the signal is 50 Ω.

The calibrated RJ modulation range is 0 to 0.025 UI-rms. However, if a filter is inserted in the RJ path, then the modulation amplitude will be attenuated by the insertion loss and bandwidth of the filter. For this reason, the user can program the RJ modulation amplitude to a maximum of 0.150 UI-rms. However, RJ is uncalibrated above 0.025 mUI.

NOTE The RJ is settable to as low as 0 UI-rms. However, each N4960A-CJ1 will have its own intrinsic RJ minimum, below which, the system cannot achieve the desired value. Typically, this lower limit is between 5 to 12 mUI-rms. It is suggested that the intrinsic RJ be checked for operation in the intended application.

The SJ1, SJ2, random jitter, and external low deviation settings can be controlled programmatically or through the front panel.

3.15.5 Low Frequency Band Periodic or External Jitter Path

A second modulation path is available for low frequency (high deviation) stress injection. It can only be operated when all of the high frequency band (low deviation) stress sources (SJ1, SJ2, RJ, and external low deviation) are disabled. The low band path operates over lower modulation frequencies, up to 17 MHz (using internal PJ), or up to 4 MHz (external). The modulation source can be either an internally generated sinusoid (Periodic Jitter, or PJ), or externally supplied through the Ext Jitter In connector. Externally applied low band jitter must have a sinusoidal wave shape. Both internal and external jitter modulation amplitude decreases as a function of modulation frequency. Refer to 5 Performance Specifications for exact ranges.

NOTE Enabling periodic jitter or external low band jitter enables the low frequency band path (the low frequency band is the default path). Enabling SJ1, SJ2, random jitter, or external high frequency band enables the high frequency band path. Switching between low frequency band and high frequency band jitter sources or between jitter sources within the same band may cause a phase shift in the jittered clock and the pattern generator. Before performing measurements, enable the jitter source to be used for the measurement, set the amplitude to 0 UI then perform an auto alignment.

NOTE Applying excessive amplitude to the external jitter input will overdrive the modulation driver, resulting in non-linear operation or intermittent output (clock slips). The instrument does not detect an external modulation overdrive condition.

3.15.6 Spread Spectrum Clock Modulation (N4960A-CJ1 only)

The main synthesizer in the N4960A-CJ1 controller can be modulated to enable spread spectrum clocking (SSC). Spread spectrum clocking is not generally considered to be a stress, but rather a method of controlling electromagnetic interference (EMI), by spreading the peak energy of the system clock over a broad portion of the spectrum. In practice, SSC modulates the system clock in the device with a large phase deviation at a relatively low frequency, generally 30 or 33 kHz. The modulation wave shape is usually triangle, to keep the power spectrum even over the modulation band. To emulate a transmitter of a device employing SSC, the clock synthesizers used in BERTs include SSC. To assure proper tracking of the BERT or sampling scope testing a device with SSC, all three clock outputs of the N4960A-CJ1 controller (Jittered, Delayed and Divided) are modulated with the same SSC signal. The SSC deviation range is 0 – 1%[1]. The modulation envelope is a triangle waveform. The modulation frequency can be set from 1 Hz to 50 kHz. In addition, there are three settings for deviation direction: down, center and up (relative to the clock frequency setting).

The spread spectrum clock modulation settings can be controlled programmatically or through the front panel.

3.15.7 External Clock Input

The external clock input accepts an external clock to be substituted for the internal synthesizer. The supplied signal can be driven across the same frequency range as the internal synthesizer. Spread spectrum clock modulation is not available when using the external clock input.

The external clock input can be enabled or disabled programmatically or through the front panel.

NOTE **Setting the clock source to External with no signal applied to the Ext Clock In connector will result in unstable operation.**

The pattern generator and error detector remote heads incorporate half rate clock architecture. When used as a BERT, any externally supplied clock input must be at 1/2 the desired data rate.

[1] (1% = 10,000 ppm)

3.15.8 Delayed Clock Input

The front panel Delayed Clk In allows users to employ an alternate clock source in the delay path. For an error detector, this may be desired when used with a clock recovery device. For a pattern generator connected to the Delay port, this may be useful to provide an asynchronous clock for a generator used as an aggressor in cross talk testing.

By default, the delay clock and error detector/pattern generator clock are sourced from the main synthesizer (refer to Figure 16 or Figure 17, block diagram). When the External Delay Clock input is used to source a different clock, the instrument needs to know the external delay clock frequency to assure proper operation.The user must enter the correct external delay clock rate. When no value is entered, the instrument defaults to the frequency of the clock used in the main clock path.

Because the error detector and pattern generator remote heads incorporate a half rate clock architecture, any externally applied clock to the Delay Clock In must be at one half the desired data rate for the error detector or pattern generator. Some clock recovery units generate half-rate clock outputs. If this is not the case, use an external divide by two clock divider to provide the correct clock frequency.

NOTE

If the Delayed Clock In is set to External to drive the Delay Clock Outputs of the N4960A and the clock source is set to External, a valid clock signal MUST be applied to the Ext Clock In connector for the Delay Clock Outputs to function properly.

3.15.9 N4960A Serial BERT Controller Output Stages

The three clock outputs are AC coupled. Certain devices will not function properly and cannot be connected to AC coupled equipment unless an offset and termination voltage can be applied to the signal. To meet these requirements, each output stage has an integrated bias tee.

On each output of the N4960A serial BERT controller, the amplitude, offset voltage, termination voltage, and AC/DC coupling can be set independently. These settings affect the signal at the Jitter, Delay, and Divided front panel output connectors. The signals driven into the pattern generator and error detector are not affected by these settings. Before setting termination voltage and offset voltage, DC coupling must be selected. Figure 14 is a simplified diagram of the N4960A serial BERT controller output stages.

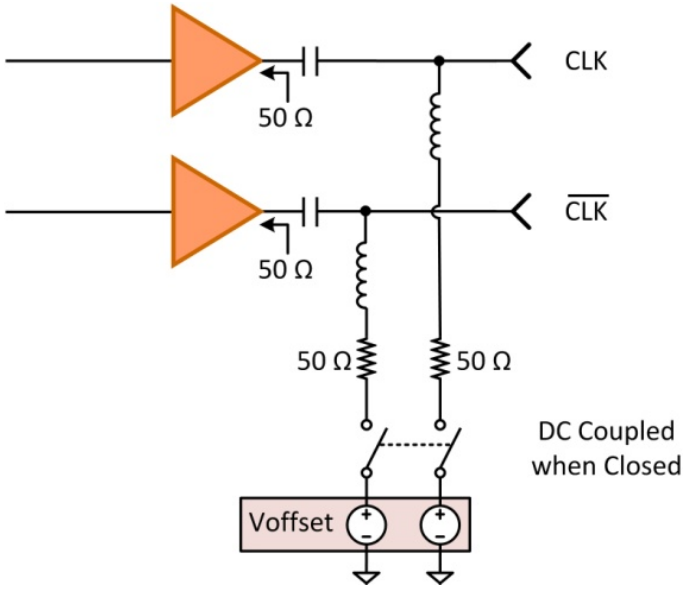


Figure 20. N4960A serial BERT controller output stages

3.16 Pattern Generator

The pattern generator utilizes a half rate clock architecture that enables patterns to be generated at data rates from 5 to 32 Gb/s or 4 to 17 Gb/s. The differential output has fully adjustable output amplitude, crossover, termination, and DC offset.

All features can be controlled through the control panel on the front panel of the N4960A serial BERT controller, remote SCPI commands, or through the N4980A multi-instrument BERT software.

3.16.1 Library of Patterns

Provided with the pattern generator is a large library of common stress patterns:

- Family of hardware generated PRBS patterns (2n – 1, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51)
- Clock patterns (÷2, ÷4, ÷8,..., ÷64)
- K28 series patterns (K28.3, K28.5, K28.7)
- CJ series patterns (CJPAT, CJTPAT, CRPAT)
- JSPAT and JTSPAT patterns

Pattern inversion is available for all patterns.

3.16.2 Programmable Patterns

The pattern generator allows custom designed patterns from 1 bit – 8 Mbit memory depth to be created and uploaded to meet application requirements. User patterns must fit into the internal 512-bit memory boundary; therefore, all odd-length patterns will be replicated 512 times before loading into the N4960A, and even-length patterns will be replicated between 1 and 256 times (depending on the actual length of the pattern). Patterns are created and loaded into the N4960A Serial BERT using the N4980A Multi-instrument BERT Software package; the pattern editor in this software performs the necessary replication calculations and will advise the user of any patterns that will not fit into the 8 Mb memory (after replication) along with suggestions on the nearest pattern lengths that will fit.

The N4980A multi-instrument BERT software enables users to create their own unique patterns, and has several built-in tools to facilitate pattern creation. A library of factory and utility patterns is provided, such as
PRBS and clock patterns, which can be used in conjunction with custom designed patterns in any combination to create complex patterns. Users have a number of editing tools at their disposal, such as viewing the pattern as a waveform, inverting a selection of bits, and finding a sequence of bits or the longest run of ones or zeroes, all in an attempt to assist users in what can be a tedious task.

For more information, refer to the N4980A multi-instrument BERT software user guide.

3.16.3 Error Injection

The error injection feature can be configured either to inject a single error or inject errors at a specified rate. Error injection is commonly used to verify that the device under test (DUT) setup is correct when in a loop back configuration.

A single error can be injected whether the error injection feature is enabled or not. When the **ErrInjSingle** command is highlighted in the **Pattern Menu**, the **EXEC** softkey is selected to inject a single error.

Errors can also be injected at specified rates from 10^{-3} to 10^{-9} using the **ErrInjRate** command in the **Pattern Menu**. For example, if 10^{-3} is selected, a single error is injected approximately every thousand bits.

Error injection can also be controlled using the corresponding remote SCPI commands.

3.16.4 Pattern Generator Output Stage

The output of the pattern generator has its own amplitude, offset, and termination voltage settings. However, there is no switch between AC and DC coupling. The DC offset and termination paths are always active but default to 0 V. Pre-defined settings allow the user to easily select industry standard logic levels including ECL, LVPECL, and LVDS. The termination voltage is used to meet the requirements of an external device. Figure 21 is a simplified diagram of the pattern generator output stage.

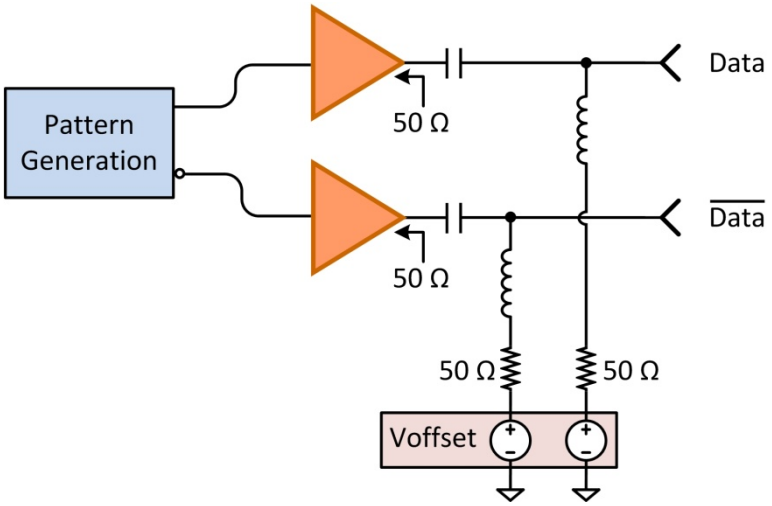


Figure 21. Pattern generator output stage

3.16.5 Dual Pattern Generator Operation

Two pattern generators can be configured for dual channel pattern generation with delay control for lane alignment.

In this configuration, the pattern generators have independent controls that are identical except for jitter injection and delay control. Refer to Figure 36. Jitter injection is applied to the pattern generator connected to the Jitter connector only.

In order to send remote commands to the intended pattern generator, [(@<channel list>)] defines which channel(s) to apply the command. Channel 0 is the jitter channel and channel 1 is the delay channel. Refer to 6.8 Pattern Generator Channelization.

Dual pattern generators can also be controlled using the N4980A multi-instrument BERT software.

3.16.6 N4951B-D17/-D32 Pattern Generator with 5-tap De-emphasis

The N4951B de-emphasis options provide integrated 5-tap de-emphasis (1 pre-cursor, 2 post cursors) and are available in 17 Gb/s and 32 Gb/s versions. The de-emphasis head provides designers with the signal pre-distortion capability required for transmitter emulation when characterizing receivers, backplanes, and systems.

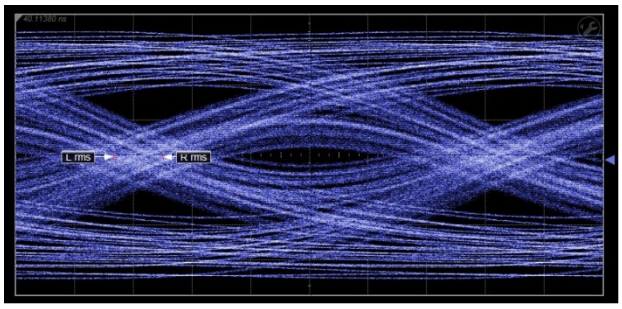


Figure 22. No de-emphasis

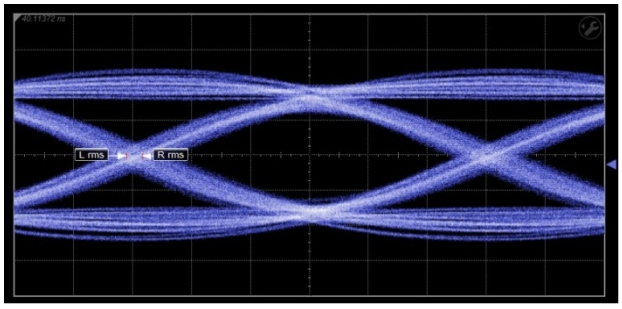


Figure 23. De-emphasis equalization applied

The taps can be adjusted from the front panel of the N4960A, using the Deemphasis functions in the Pat Gen-Jit Menu, or the N4980A multi-instrument BERT software.

The N4980A includes a de-emphasis tap weight computation tool that simplifies the process of computing tap weights into the following steps:

1. Load a measured or simulated s-parameter file of the channel loss.
2. Click on the start calculation button (blue button). The software calculates the minimum tap values necessary to create the ideal compensation filter response.
3. Fine tune the taps if necessary for optimal fit.
4. Select the pattern generator with de-emphasis.
5. Click on the Set Taps button to load the computed tap weights into the N4951B-D17/-D32 pattern generator head.

For more information about the N4980A de-emphasis tap weight calculator, refer to the N4980A multi-instrument BERT software user guide.

3.17 Error Detector

The error detector utilizes a half rate clock architecture that enables error detection at data rates from 5 to 32 Gb/s or 4 to 17 Gb/s. The differential output has adjustable input termination voltage.

All features can be controlled through the control panel on the front panel of the N4960A serial BERT controller, remote SCPI commands, or through the N4980A multi-instrument BERT software.

3.17.1 Error Detector Input Stage

The input comparator of the error detector is AC coupled, with programmable DC termination voltage. The termination voltage is always active, but the default value is 0 V. Figure 24 is a simplified diagram of the error detector input stage.

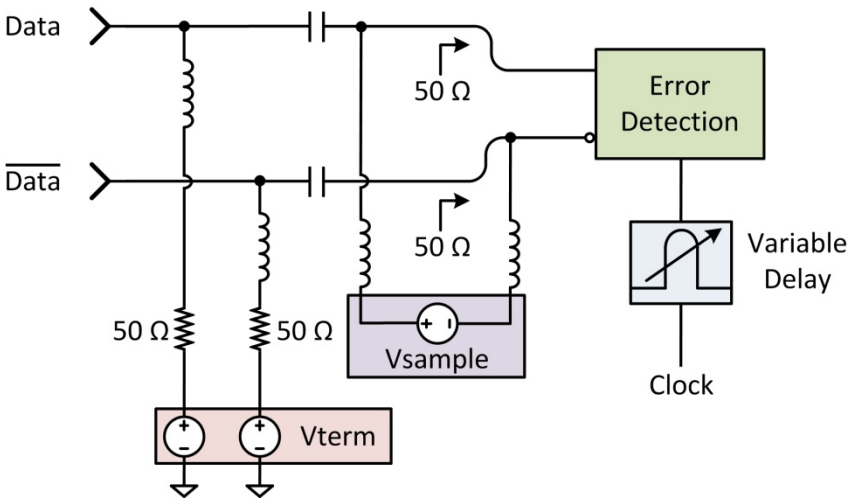


Figure 24. Error detector input stage

3.17.2 Pattern Selection

Patterns are identical to those available for use with the pattern generator. A pattern must first be selected before synchronization can be attempted.

3.17.3 Synchronization

Synchronization is the process of bit aligning the detector internal reference pattern with the input bit stream. Synchronization can be initiated automatically or manually. Synchronization can be impacted by several factors, including the detector decision point. The decision point should be set appropriately for the test setup before synchronization is attempted. The decision point can be automatically adjusted by the error detector. However, if the eye is considerably closed from excessive jitter or Inter Symbol Interference, the user may need to manually perform the initial alignment.

In auto mode, synchronization can be configured to occur when a specified BER threshold has been reached using the BER Thrshld command in the Sync Menu. The default mode is auto synchronization. Auto synchronization can also be controlled using the corresponding remote SCPI commands.

Changing the Sync Mode to Manual allows synchronization to be performed each time the Sync Now command is executed in the Sync Menu. Manual synchronization can also be initiated using the corresponding remote SCPI commands.

3.17.4 Auto Pattern

When the Auto Pattern feature is enabled, Pat Type is set to PRBS and the error detector automatically detects and synchronizes to PRBS patterns. If Auto Pattern cannot determine the pattern type, the message “Unknown” is displayed.

3.17.5 Alignment

Alignment is the process which places the detector decision point in the optimal position in the eye. The two parameters which position the detector are time (delay) and amplitude (sample threshold voltage). The time (delay) parameter positions the decision point horizontally while the amplitude (sample threshold voltage) parameter positions the decision point vertically. Alignment can be done either automatically or manually.

In auto mode, the sample threshold voltage and delay step size are configured using the Config AutoAlign command in the AutoAlign Menu. In addition, Set SmplV (sample voltage) and Set Delay (delay) must be enabled (ON). The default for Set SmplV and Set Delay is enabled. The auto alignment is performed by executing the Perform AutoAlign command. After the auto alignment is performed, the results can be viewed which includes eye height and eye width. Auto alignment can also be controlled using the corresponding remote SCPI commands.

In manual mode, the sample voltage and delay can be adjusted using SmplV and Delay in the Input Adjust menu. Manual alignment can also be controlled using the corresponding remote SCPI commands.

NOTE

Use of auto-align with memory based patterns (.fpt or .usr) is not recommended because it can be quite slow depending on the pattern length. Instead, perform auto-align on a hardware PRBS pattern then switch to the memory based pattern. Changing patterns does not affect alignment.

3.18 Half Rate Clock Architecture

The pattern generator and error detector utilize half rate clock architecture relative to the N4960A serial BERT controller. This means that the N4960A serial BERT controller settings for jitter, delay, and spread spectrum clock, are half that of the pattern generator and error detector settings.

Jitter and delay settings for the N4960A serial BERT controller, pattern generator, and error detector are expressed in unit intervals. A unit interval, also referred to as a bit period, is the time taken in a data stream for one bit. For example, if the data rate is set to 10 Gb/s (controller set to 5 GHz), the unit interval is 1 ÷ 10 Gb/s, which equals 100 ps, the time for one bit.

Jitter and delay unit intervals can be set at the N4960A serial BERT controller or at the pattern generator and error detector. Therefore, it is important to understand the relationship between the clock outputs (N4960-CJ0/N4960-CJ1), the pattern generator, and the error detector as described in the following sections.

NOTE

When using remote SCPI commands, jitter, delay, and spread spectrum clock can only be set at the N4960A serial BERT controller. Therefore, SCPI values related to UI, such as jitter amplitude or delay, must be set to half of the value desired on the pattern generator outputs or error detector delay.

3.18.1 Jitter Relationship Between Clock Output and Pattern Generator Output

Figure 25 illustrates the jittered clock output from the N4960A serial BERT controller relative to the jittered output of a pattern generator connected to the Jitter port. Note that one clock period corresponds to two bit periods. With SJ amplitude set to 0.1 UI in the N4960A serial BERT controller, the SJ amplitude of the pattern generator will be set to 0.2 UI automatically. Conversely, if the SJ amplitude of the pattern generator is set to 0.2 UI, the SJ amplitude of the N4960A serial BERT controller will be set to 0.1 UI automatically.

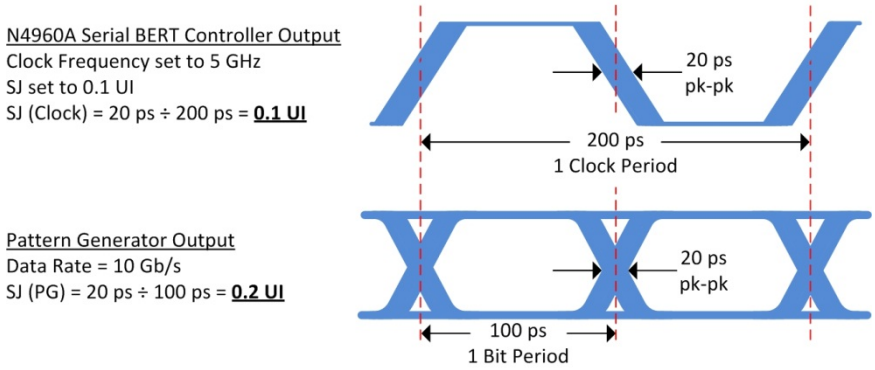


Figure 25. Jitter relationship

3.18.2 Delay Relationship Between Remote Head and Delay Clock Output

Figure 26 illustrates the delayed clock output from the N4960A serial BERT controller relative to the delay of a pattern generator or error detector connected to the Delay port. Note that one clock period corresponds to two bit periods. With the delay set to 0.1 UI in the N4960A serial BERT controller, the delay of the pattern generator/error detector will be set to 0.2 UI automatically. Conversely, if the delay of the pattern generator/error detector is set to 0.2 UI, the delay of the N4960A serial BERT controller will be set to 0.1 UI automatically.

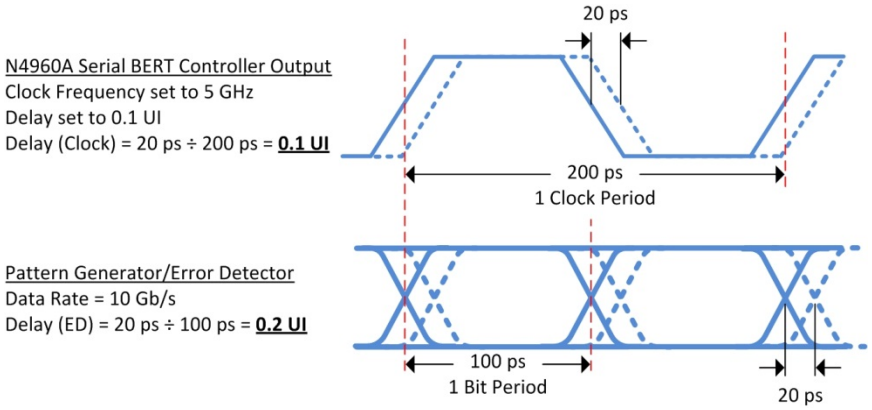


Figure 26. Delay relationship

3.19 Bit Error Rate Tests

A bit error rate (BER) test is performed by driving the pattern generator output into a DUT and back into the input of the error detector. Each bit of the detector internal reference pattern is compared to the input bit stream, and each mismatch is recorded as an error. The BER represents the ratio of total number errors detected to total number of bits received. For example, 1 error bit out of 1,000,000 total bits would result in a BER of 1e-6 (1/1,000,000).

The N4960A serial BERT 17 and 32 Gb/s can be set up to run BER tests using the front panel, remote SCPI commands, or N4980A multi-instrument BERT software.

3.19.1 Setting up a Basic BER Test

Regardless of the method used to set up a BER test, the following describes the setup requirements.

1. Set the clock frequency and pattern generator data rate.

   The pattern generator data rate is based on the clock frequency setting. Due to the half rate clock architecture of the remote heads, the clock frequency setting is half that of the remote heads.

2. Set the pattern generator logic level.

   The data logic level sets the amplitude, offset, and termination voltages appropriate for the DUT. Logic level choices include ECL, LVPECL, and LVDS. Entering values other than ECL, LVPECL, or LVDS values are considered “custom” entries.

3. Select a pattern.

   For most devices which use conventional loop back, the pattern generator and error detector patterns must match.

4. Enable the pattern generator output.

   The pattern generator output defaults to disabled. Therefore, ensure that the output is enabled. This is done using the Enable function in the Data Output Menu (within the Pattern Gen Menu).

5. Synchronize the error detector.

   Synchronize the error detector internal reference pattern with the input bit stream. This may be done automatically or manually.

6. Align the error detector.

   The time (delay) parameter positions the decision point horizontally while the amplitude (sample voltage) parameter positions the decision point vertically. This may be done automatically or manually.

7. Set the BER measurement criteria.

   Set the criteria for a BER test based on duration, number of bits, or number of errors. The BER test can also be set to start/stop manually.

8. Start the BER measurement (accumulation).

3.19.2 Accumulated and Instantaneous BER

The accumulated BER (aBER) tracks the currently accumulated bit error rate, the total number of errors, the total number of logic 1 errors, the total number of logic 0 errors, and the elapsed time. If the aBER is cleared after the accumulation has stopped, all numbers are reset.

The instantaneous BER (iBER) displays the BER at the current instant in time. The iBER is updated at a constant rate, regardless of whether an accumulated BER test is running.

3.20 Control Panel Operation

This section describes how to use the Control Panel to operate the N4960A serial BERT 17 and 32 Gb/s. Refer to Figure 27.

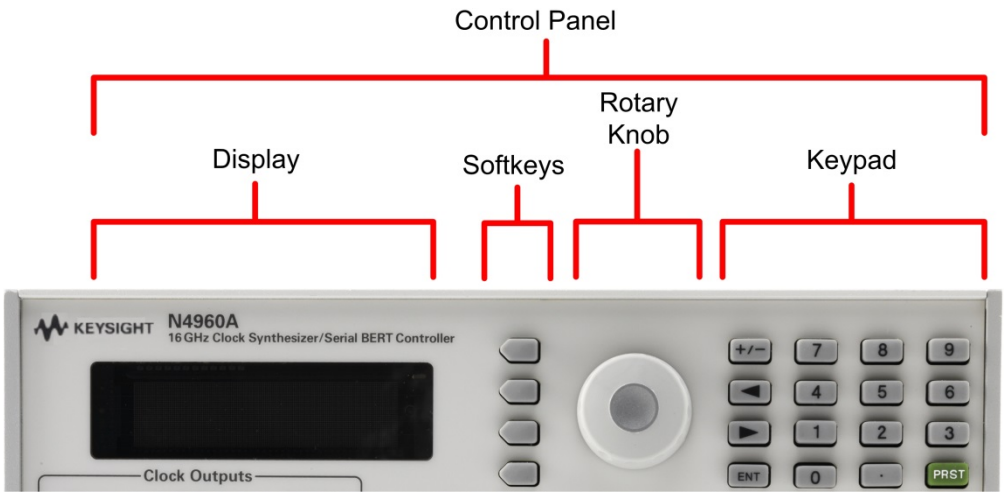


Figure 27. Control panel

3.20.1 Menu Navigation

Navigation through the menus is accomplished with the four softkeys to the right of the display and the rotary knob. Refer to Figure 28.

Figure 28. Softkey navigation buttons and rotary knob

Scroll through menu items using either the softkeys corresponding to the up and down arrow labels, or using the rotary knob. Refer to Figure 29.

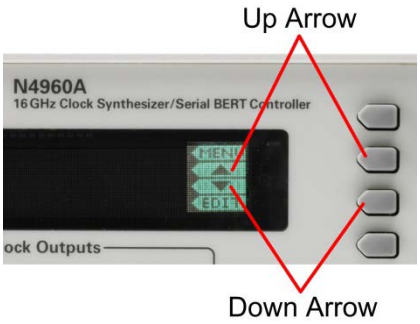


Figure 29. Scrolling through menu items

If a menu item has a lower-level menu that can be accessed, the SEL softkey appears. Press it to access the corresponding lower-level menu. Refer to Figure 30.

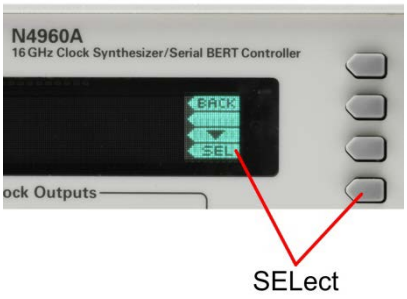


Figure 30. Accessing lower-level menus

3.20.2 Changing Parameters

The **EDIT** label appears when a menu item has a numeric value that can be changed or has multiple selections (for example, on and off). Refer to Figure 31.

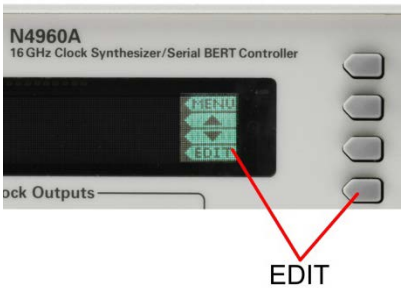


Figure 31. EDIT label

When the softkey corresponding to the **EDIT** label is pressed, the function's parameter can be changed using the rotary knob or the keypad.

NOTE **The keypad is used if a parameter is a numeric value only.**

Figure 32 is an example of changing parameters using the rotary knob.

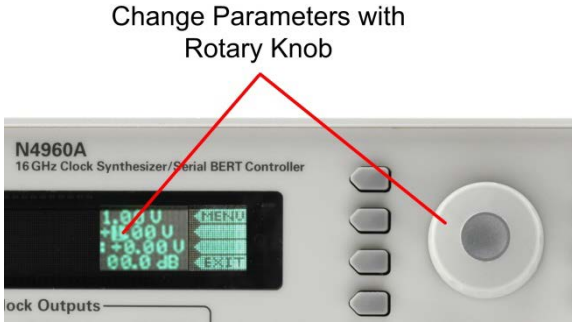


Figure 32. Changing parameters using the rotary knob

If you are using the rotary knob to change numeric values, use the right/left arrows on the keypad to highlight the digit you wish to change. The right arrow highlights the digit to the right. The left arrow highlights the digit to the left. When finished, press the softkey corresponding to the EXIT label to return to the previous screen. Refer to Figure 33.

Figure 33. Highlighting digits to change

NOTE When using the rotary knob, changes to numeric values occur instantly. This applies to almost all numeric values.

In addition to the rotary knob, the numeric keypad can be used to change numeric values. Once the softkey corresponding to the EDIT label is pressed, simply enter the value using the numeric keypad. When finished, either press the ENT hardkey on the keypad, or press the softkey corresponding to the associated units label to accept the entry. Refer to Figure 34.

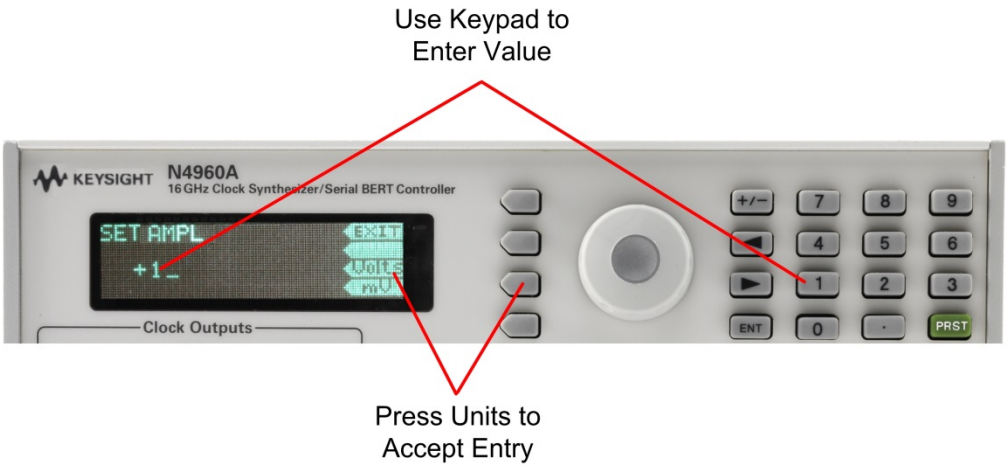
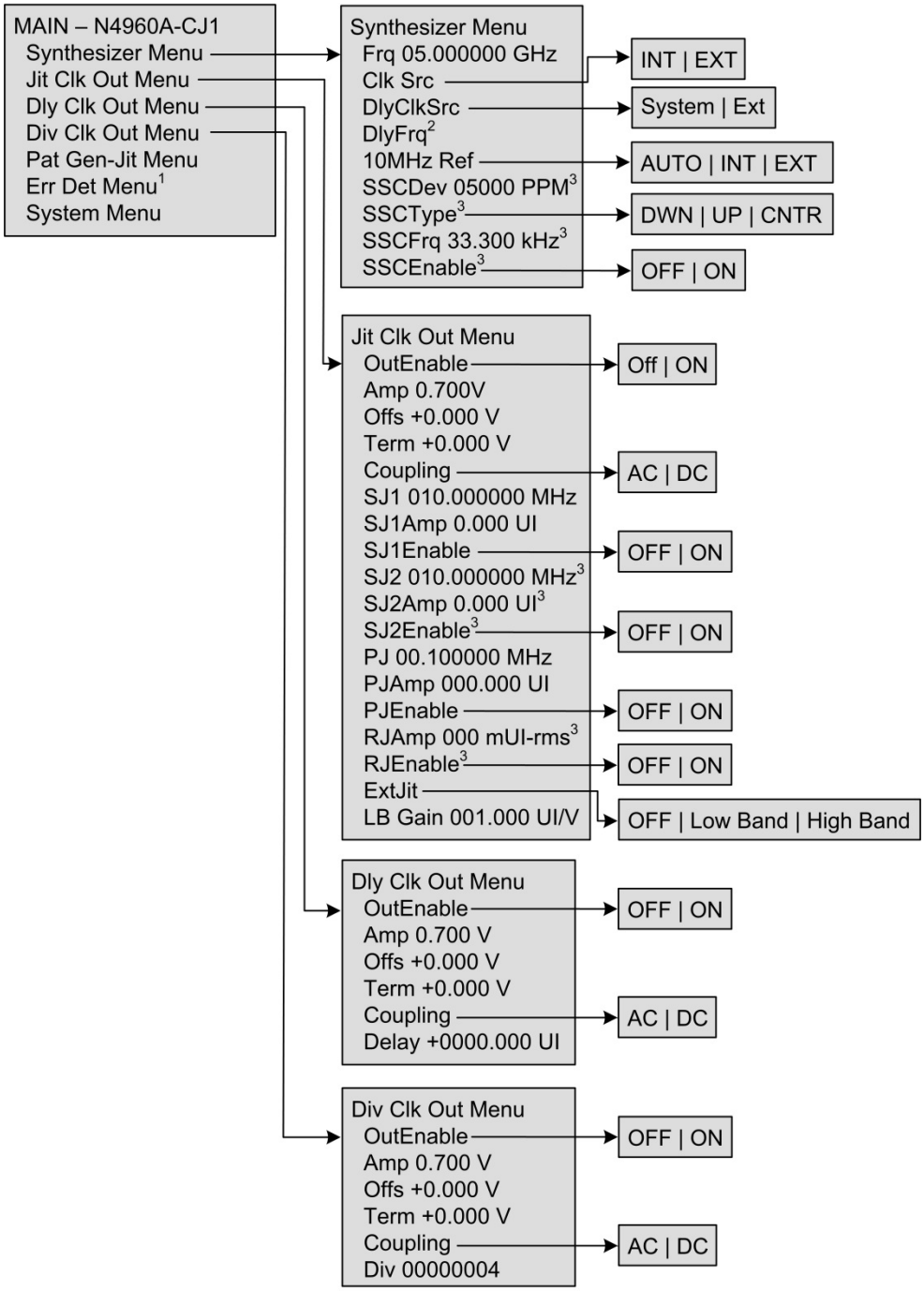


Figure 34. Using the numeric keypad

NOTE When changing values using the numeric keys, the change is not accepted until the **ENT** hardkey in the keypad, or a unit softkey is pressed.

3.20.3 Menu Structure

Figure 35 shows the hierarchical structure of the Synthesizer, Jitter, Delay, and Divided menus. Note that some parameters such as data rate and jitter control, appear in both the synthesizer and the pattern generator menus. This is to accommodate the half rate clock of the pattern generator and error detector. When entered in the synthesizer menu, the values correspond to the clock outputs on the front panel. When entered in the pattern generator menu, the 2X conversion factor is automatically applied so the values correspond to the pattern generator output.



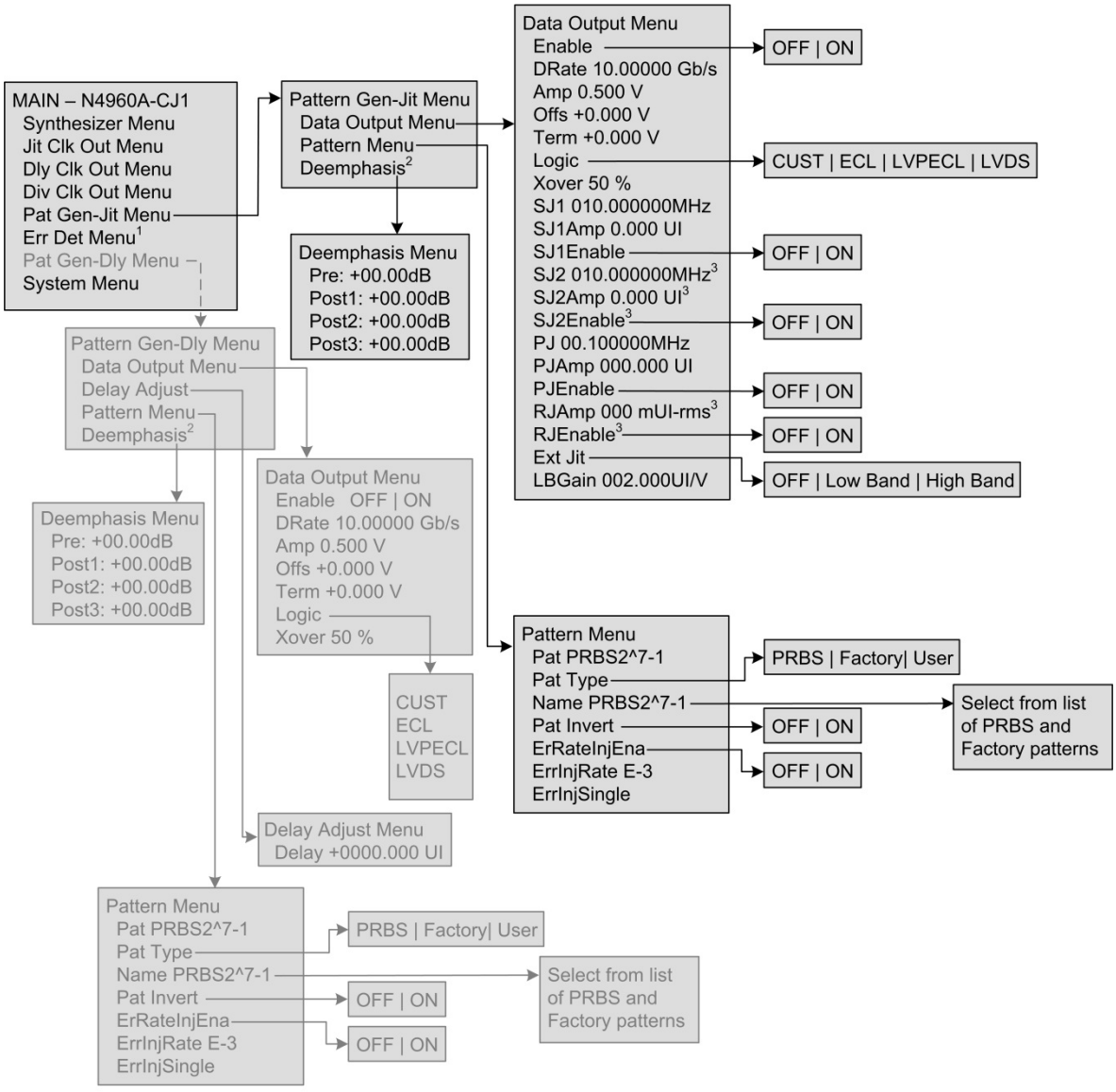
[1] The label changes to Pat Gen-Dly Menu when a pattern generator is connected to the Delay connector on the front panel of the N4960A.

[2] Displays See Frq when DlyClkSrc set to System. When DlyClkSrc set to Ext the frequency can be set.

[3] Feature available in N4960A-CJ1 only.

Figure 35. Synthesizer, jitter, delay, and divided menu structure

Figure 36 shows the hierarchical structure of the pattern generator menus.



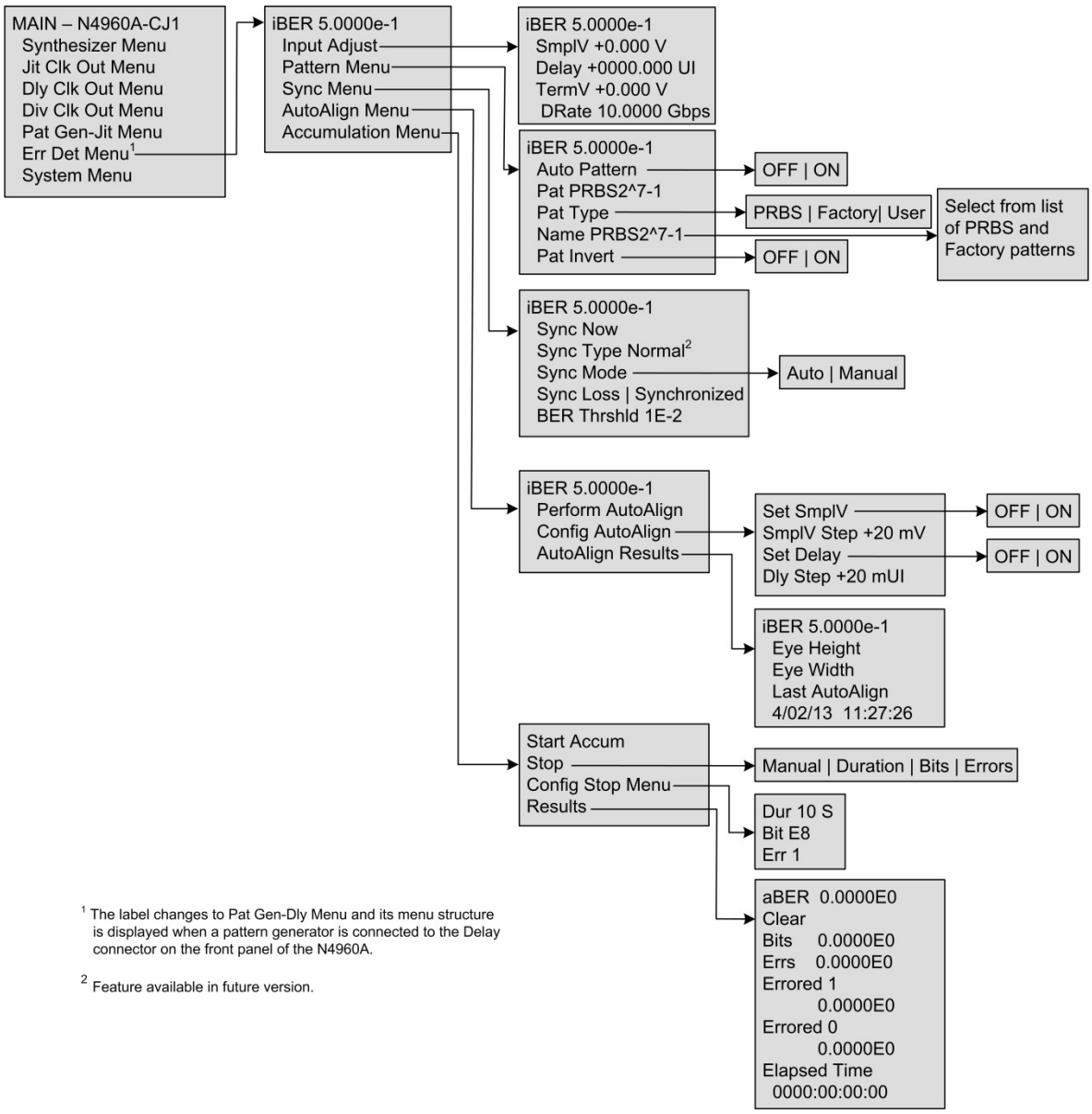
[1] The Err Det Menu label changes to Pat Gen-Dly Menu and its menu structure is displayed when a pattern generator is connected to the Delay connector on the front panel of the N4960A.

[2] Deemphasis available on N4951B-D17/-D32 pattern generators only.

[3] Feature available in N4960A-CJ1 only.

Figure 36. Pattern generator menu structure

Figure 37 shows the hierarchical structure of the error detector menus.



[1] The label changes to Pat Gen-Dly Menu and its menu structure is displayed when a pattern generator is connected to the Delay connector on the front panel of the N4960A.

[2] Feature available in future version.

Figure 37. Error detector menu structure

Figure 38 shows the hierarchical structure of the System menus.

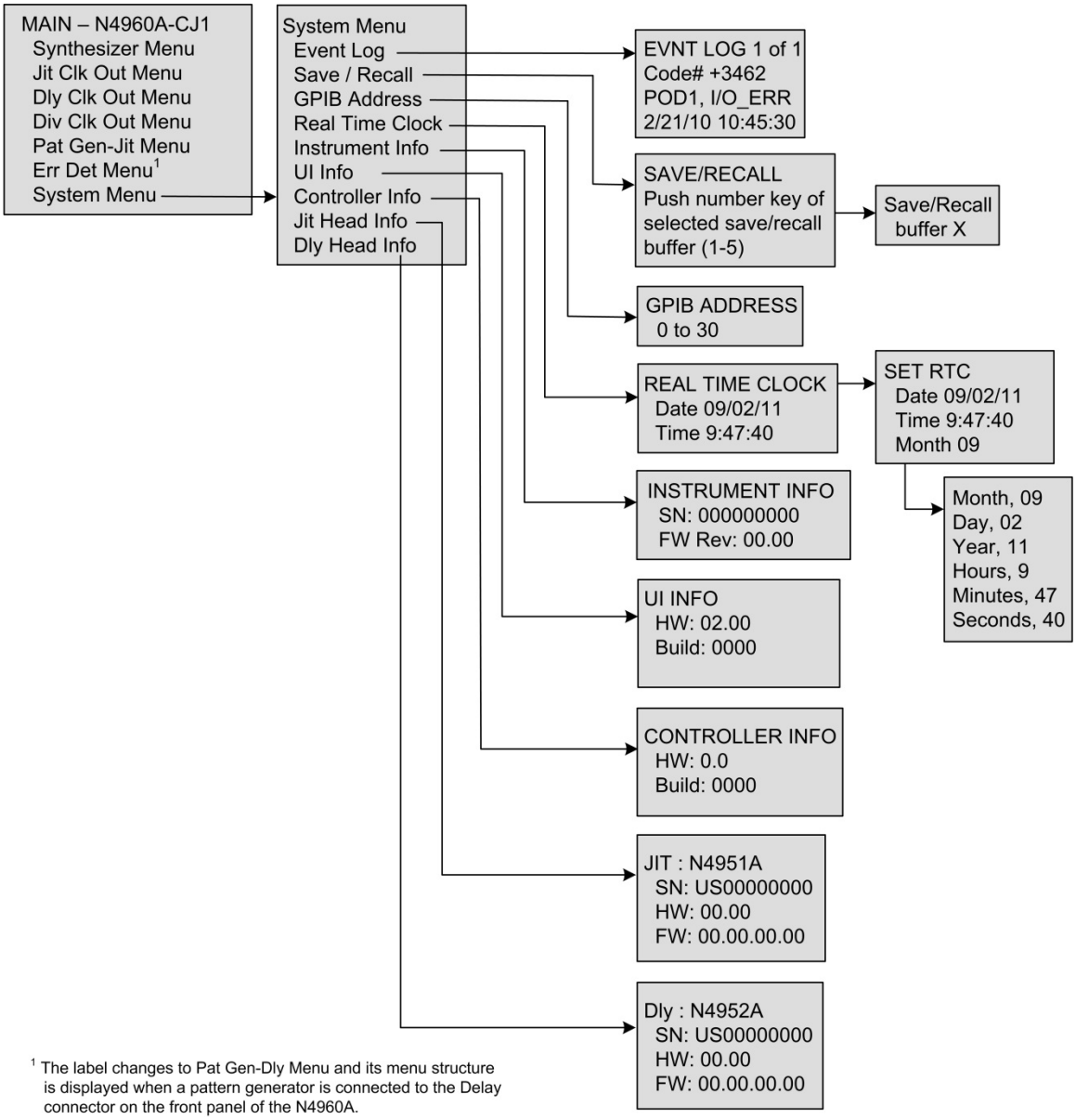


Figure 38. System menu structure

3.20.4 Menu Label Descriptions

Refer to Table 14 for the Synthesizer Menu descriptions.

Table 14. Synthesizer Menu descriptions

Label Name	Description
Frq	Sets the clock source frequency. The optional units are kHz, MHz, and GHz. The resolution is 1 kHz. Displays EXTERNAL when External clock source is selected.
ClkSrc	Sets the clock source to INT for using the internal clock source or EXT for using an external clock source. SSC cannot be enabled if the clock source is external. If the SSC enabled state conflicts with the clock source, a message indicating a conflict appears in the N4960A-CJ1 controller display. Selecting Yes to resolve the conflict will set the SSC enabled state to an appropriate value.
DlyClkSrc	Sets the delay clock to be System for using the internal delay clock, or Ext for using an external delay clock. Setting the DlyClkSrc to System will use either the internal synthesizer or the external clock, whichever ClkSrc is set to.
DlyFrq	Sets the delay clock frequency when DlyClkSrc is set to Ext. When DlyClkSrc is set to System, the message “See Frq” is displayed referring to the frequency of the system clock.
10MHzRef	Sets the 10 MHz reference to INT for using the internal 10 MHz reference, EXT for using an external 10 MHz reference, or AUTO for detecting and connecting to an external reference automatically.
SSCDev[1]	Sets the spread spectrum clock deviation. The units are PPM (parts per million). The resolution is 1 PPM.
SSCType[1]	Sets the spread spectrum clock deviation direction from down (DWN) spread, up (UP) spread, or center (CNTR) spread.
SSCFrq[1]	Sets the spread spectrum clock frequency. The optional units are Hz and kHz. The resolution is 1 Hz.
SSCEnable[1]	Enables/disables the spread spectrum clock function. SSC cannot be enabled if the clock source is external. If the clock source conflicts with the SSC enabled state, a message indicating a conflict appears in the N4960A-CJ1 controller display. Selecting Yes to resolve the conflict will set the clock source to an appropriate value.

[1] Feature available in N4960A-CJ1 only.

NOTE If the clock source is set to External without a valid clock signal connected, then the results from the :SOUR:FREQ? query may fluctuate or return “0000 Hz”. In addition, a “FREQ/OOR” (frequency out of range) error may be generated. If either of these conditions is detected, check the external clock source.

NOTE If the 10 MHz Reference is set to Auto mode, whenever it switches between Internal and External, a message indicating the switch is generated (“REF,INTERNAL” and “REF,EXTERNAL”) respectively. If the 10 MHz Reference is using an External source and there is a loss of signal, a loss of signal error will be generated (“REF,LOS”).

Refer to Table 15 for the Jit Clk Out menu descriptions.

Table 15. Jit Clk Out menu descriptions

Label Name	Description
OutEnable	Enables/disables the jittered clock output.
Amp	Sets the amplitude of the jittered clock. The optional units are mV and V. The resolution is 0.005 V.
Offs	Sets the offset of the jittered clock. The maximum range is a function of the termination voltage setting. The optional units are mV and V. The resolution is 0.005 V. The offset may be limited by the current termination voltage. If the desired offset value conflicts with the current termination value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the termination to an appropriate value.
Term	Sets the termination voltage of the jittered clock. The maximum range is a function of the offset setting. The optional units are mV and V. The resolution is 0.005 V. The termination may be limited by the current offset voltage. If the termination value conflicts with the offset value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the offset to an appropriate value.
Coupling	Selects AC or DC output coupling. Coupling must be set to DC before offset or termination can be set to a non-zero value. If an attempt to change the offset or termination to a non-zero value conflicts with the AC coupling setting, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the coupling to DC.
SJ1	Sets the sinusoidal jitter 1 frequency. The optional units are Hz and MHz. The resolution is 1 Hz.

Label Name	Description
SJ1Amp[2]	Sets the sinusoidal jitter 1 amplitude. The optional units are mUI and UI (p-p). The resolution is 0.001 UI. During the setting of SJ1 amplitude, if SJ1 and/or SJ2/RJ are enabled simultaneously, keep the sum of all 3 components below the specified maximum modulation level.
SJ1Enable	Enables/disables the sinusoidal jitter 1. SJ1 cannot be enabled if PJ or external jitter (low band) is enabled. If the SJ1 enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.
SJ2[1]	Sets the sinusoidal jitter 2 frequency. The optional units are Hz and MHz. The resolution is 1 Hz.
SJ2Amp[1,2]	Sets the sinusoidal jitter 2 amplitude. The optional units are mUI and UI (p-p). The resolution is 0.001 UI. During the setting of SJ1 amplitude, if SJ1 and/or SJ2/RJ are enabled simultaneously, keep the sum of all 3 components below the specified maximum modulation level.
SJ2Enable[1]	Enables/disables the sinusoidal jitter 2. SJ2 cannot be enabled if PJ or external jitter (low band) is enabled. If the SJ2 enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the N4960A-CJ1 controller display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.
PJ	Sets the periodic jitter frequency. The optional units are Hz and MHz. The resolution is 1 Hz. The maximum PJ amplitude is a function of PJ frequency. If the PJ frequency conflicts with the current PJ amplitude, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set PJ amplitude to an appropriate value.
PJAmp	Sets the periodic jitter amplitude. The optional units are mUI and UI (p-p). The resolution is 0.001 UI. The maximum PJ amplitude is a function of PJ frequency.

Label Name	Description
PJEnable	Enables/disables the periodic jitter. Periodic Jitter cannot be enabled if any other internal or external jitter source is enabled. If the PJ enabled state conflicts with other jitter sources, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will disable all other jitter sources.
RJAmp[1]	Sets the random jitter amplitude in RMS. The optional units are mUI-rms and UI-rms. The resolution is 1 mUI-rms. The maximum calibrated RJ amplitude is 25 mUI-rms, but the system allows values up to 150 mUI-rms to offset any amplitude loss caused by use of a filter on the RJ input. When used in combination with other high frequency band stresses (SJ1, SJ2, and external high band jitter), keep the sum of all 3 components below the specified maximum modulation level.
RJEnable[1]	Enables/disables the random jitter output. RJ cannot be enabled if PJ or external jitter (low band) is enabled. If the RJ enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the N4960A-CJ1 controller display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.
ExtJit	Selects the external jitter input path. High band external jitter can be enabled in combination with SJ1, SJ2, and RJ. Low band external jitter cannot be enabled if any other jitter source is enabled. If the low band external jitter enabled state conflicts with other jitter sources, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will disable all other jitter sources.
LB Gain	Sets the gain of the external low band gain. The optional units are mUI/V or UI/V.

[1] Feature available in N4960A-CJ1 only.

[2] Note that the sum of SJ1, SJ2, RJ, and external jitter low deviation amplitude should not exceed the specified maximum deviation. However, the system only checks SJ1 and SJ2.

NOTE

Sinusoidal 1 jitter, Sinusoidal 2 jitter, random jitter, and external jitter high frequency band (low deviation) can be enabled simultaneously. However, when used in combination, make sure that the sum of these paths does not exceed the specified maximum modulation level. In addition, periodic jitter or external low band jitter cannot be enabled if any of the other jitter paths are enabled.

Refer to Table 16 for the Dly Clk Out menu descriptions.

Table 16. Dly Clk Out menu descriptions

Label Name	Description
OutEnable	Enables/disables the delayed clock output.
Amp	Sets the amplitude of the delayed clock. The optional units are mV and V. The resolution is 0.005 V.
Offs	Sets the offset of the delayed clock. The maximum range is a function of the termination voltage setting. The optional units are mV and V. The resolution is 0.005 V. The offset may be limited by the current termination voltage. If the desired offset value conflicts with the current termination value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the termination to an appropriate value.
Term	Sets the termination voltage of the delayed clock. The maximum range is a function of the offset setting. The optional units are mV and V. The resolution is 0.005 V. The termination may be limited by the current offset voltage. If the termination value conflicts with the offset value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the offset to an appropriate value.
Coupling	Selects AC or DC output coupling. Coupling must be set to DC before offset or termination can be set to a non-zero value. If an attempt to change the offset or termination to a non-zero value conflicts with the AC coupling setting, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the coupling to DC.
Delay	Sets the delay of the delayed clock. The optional units are mUI and UI. The resolution is 0.001 UI.

Refer to Table 17 for the Div Clk Out menu descriptions.

Table 17. Div Clk Out menu descriptions

Label Name	Description
OutEnable	Enables/disables the divided clock output.
Amp	Sets the amplitude of the divided clock. The optional units are mV and V. The resolution is 0.005 V.
Offs	Sets the offset of the divided clock. The maximum range is a function of the termination voltage setting. The optional units are mV and V. The resolution is 0.005 V. The offset may be limited by the current termination voltage. If the desired offset value conflicts with the current termination value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the termination to an appropriate value.
Term	Sets the termination voltage of the divided clock. The maximum range is a function of the offset setting. The optional units are mV and V. The resolution is 0.005 V. The termination may be limited by the current offset voltage. If the termination value conflicts with the offset value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the offset to an appropriate value.
Coupling	Selects AC or DC output coupling. Coupling must be set to DC before offset or termination can be set to a non-zero value. If an attempt to change the offset or termination to a non-zero value conflicts with the AC coupling setting, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the coupling to DC.
Div	Sets the divided clock divide ratio.

Refer to Table 18 for the Pattern Gen Menu descriptions for a pattern generator connected to the Jitter (Channel 0) connector.

Common settings between the synthesizer and pattern generator are superseded by the pattern generator settings. The jitter and delay settings are replicated in the pattern generator menu for the users' convenience. All jitter amplitude and delay ranges, settings, and resolutions are double that of the Jitter Clock Output, due to the half rate clock architecture of the pattern generator remote head.

Table 18. Pat Gen-Jit menu descriptions

Label Name	Description
Data Output Menu	
Enable	Enables/disables the pattern generator output.
DRate	Displays the pattern generator data rate. DRate is not settable.
Amp	Sets the pattern generator output amplitude. Resolution is 0.005 V.
Offs	Sets the DC offset of the data eye presented at the data outputs of the pattern generator. The maximum range is a function of the termination voltage setting. The optional units are mV and V. The resolution is 0.005 V. The offset may be limited by the current termination voltage. If the desired offset value conflicts with the current termination value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the termination to an appropriate value.
Term	Sets the DC output offset of the data eye to support a specified termination voltage of a DUT having a 50 Ω input port. The maximum range is a function of the offset setting. The optional units are mV and V. The resolution is 0.001 V. The termination may be limited by the current offset voltage. If the termination value conflicts with the offset value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the offset to an appropriate value.
Logic	Sets the data logic level. The levels are ECL, LVPECL, and LVDS. Editing any parameter will automatically change the logic level to “CUST” (custom).
Xover	Sets the data crossover point (percentage).
SJ1	Sets the sinusoidal jitter 1 frequency. The optional units are Hz and MHz. The resolution is 1 Hz.
SJ1Amp[2]	Sets the sinusoidal jitter 1 amplitude relative to the output of the pattern generator (which has double the amplitude range of SJ1 of the controller). The optional units are mUI and UI (p-p). The resolution is 0.002 UI. During the setting of SJ1 amplitude, if SJ1 and/or SJ2/RJ are enabled simultaneously, keep the sum of all 3 components below the specified maximum modulation level.

Label Name	Description
SJ1Enable	Enables/disables the sinusoidal jitter 1. SJ1 cannot be enabled if PJ or external jitter (low band) is enabled. If the SJ1 enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.
SJ2[1]	Sets the sinusoidal jitter 2 frequency. The optional units are Hz and MHz. The resolution is 1 Hz.
SJ2Amp[1,2]	Sets the sinusoidal jitter 2 amplitude relative to the output of the pattern generator (which has double the amplitude range of SJ2 of the controller). The optional units are mUI and UI (p-p). The resolution is 0.002 UI. During the setting of SJ1 amplitude, if SJ1 and/or SJ2/RJ are enabled simultaneously, keep the sum of all 3 components below the specified maximum modulation level.
SJ2Enable[1]	Enables/disables the sinusoidal jitter 2. SJ2 cannot be enabled if PJ or external jitter (low band) is enabled. If the SJ2 enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the N4960A-CJ1 controller display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.
PJ	Sets the periodic jitter frequency. The optional units are Hz and MHz. The resolution is 1 Hz. The maximum PJ amplitude is a function of PJ frequency. If the PJ frequency conflicts with the current PJ amplitude, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set PJ amplitude to an appropriate value.
PJAmp	Sets the periodic jitter amplitude relative to the output of the pattern generator (which has double the amplitude range of PJ of the controller). The optional units are mUI and UI (p-p). The resolution is 0.002 UI. The maximum PJ amplitude is a function of PJ frequency.

Label Name	Description
PJEnable	Enables/disables the periodic jitter on the pattern generator connected to the Jitter connector only. Periodic Jitter cannot be enabled if any other internal or external jitter source is enabled. If the PJ enabled state conflicts with other jitter sources, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will disable all other jitter sources.
RJAmp[1]	Sets the random jitter amplitude in RMS relative to the output of the pattern generator (which has double the amplitude range of RJ of the controller). The optional units are mUI-rms and UI-rms. The resolution is 2 mUI-rms. When used in combination with other high frequency band stresses (SJ1, SJ2, and external high band jitter), the sum of all jitter source amplitudes should not exceed the maximum specified modulation level.
RJEnable[1]	Enables/disables the random jitter output. RJ cannot be enabled if PJ or external jitter (low band) is enabled. If the RJ enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the N4960A-CJ1 controller display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.
ExtJit	Selects the external jitter input path. High band external jitter can be enabled in combination with SJ1, SJ2, and RJ. Low band external jitter cannot be enabled if any other jitter source is enabled. If the low band external jitter enabled state conflicts with other jitter sources, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will disable all other jitter sources.
LB Gain	Sets the gain of the external low band gain. The optional units are mUI/V or UI/V.

Label Name	Description
Pattern Menu	
Pat	Displays the current pattern name (read only). Use the Pat Type and Name menu items to select the desired pattern.
Pat Type	Sets the type for the list of selectable patterns under “Name”. Available types are PRBS, Factory, and User.
Name	Sets the pattern name from the list of patterns filtered by Pat Type.
Pat Invert	Inverts all patterns.
ErRateInjEna	Enables/disables error injection.
ErrInjRate	Sets the error injection rates from 1E-3 to 1E-9.
ErrInjSingle	Injects a single error each time the EXEC softkey is pressed.
Deemphasis[3]	
Pre	Adjusts the impulse response sample of the bit before the cursor bit.
Post1	Adjusts the impulse response sample of the first bit after the cursor bit.
Post2	Adjust the impulse response sample of the bit that is two bits after the cursor bit.
Post3	Adjust the impulse response sample of the bit that is three bits after the cursor bit.

[1] Feature available in N4960A-CJ1 for pattern generator connected to Jitter connector only.

[2] Note that the sum of SJ1, SJ2, RJ, and external jitter low deviation amplitude should not exceed the maximum specified modulation level. However, the system only checks SJ1 and SJ2.

[3] Feature available in pattern generator with de-emphasis only.

NOTE

Sinusoidal 1 jitter, Sinusoidal 2 jitter, random jitter, and external jitter high frequency band (low deviation) can be enabled simultaneously. However, when used in combination, make sure that the sum of these paths does not exceed the specified maximum modulation level. In addition, periodic jitter or external low band jitter cannot be enabled if any of the other jitter paths are enabled.

Refer to Table 19 for the Pat Gen-Dly menu descriptions for a pattern generator connected to the Delay (Channel 1) connector.

Table 19. Pat Gen-Dly menu descriptions

Label Name	Description
Data Output Menu	
Enable	Enables/disables the pattern generator output.
DRate	Displays the pattern generator data rate. DRate is not settable.
Amp	Sets the pattern generator output amplitude. Resolution is 0.005 V.
Offs	Sets the DC offset of the data eye presented at the data outputs of the pattern generator. The maximum range is a function of the termination voltage setting. The optional units are mV and V. The resolution is 0.005 V. The offset may be limited by the current termination voltage. If the desired offset value conflicts with the current termination value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the termination to an appropriate value.
Term	Sets the DC output offset of the data eye to support a specified termination voltage of a DUT having a 50 Ω input port. The maximum range is a function of the offset setting. The optional units are mV and V. The resolution is 0.001 V. The termination may be limited by the current offset voltage. If the termination value conflicts with the offset value, a message indicating a conflict appears in the N4960A serial BERT controller display. Selecting Yes to resolve the conflict will set the offset to an appropriate value.
Logic	Sets the data logic level. The levels are ECL, LVPECL, and LVDS. Editing any parameter will automatically change the logic level to “CUST” (custom).
Xover	Sets the data crossover point (percentage).
Delay Adjust	
Delay	This sets the amount the clock must be shifted when aligning the pattern generator connected to the Delay connector on the front panel of the N4960A. Resolution is 0.002 UI.
Pattern Menu	
Pat	Displays the current pattern name (read only). Use the Pat Type and Name menu items to select the desired pattern.
Pat Type	Sets the type for the list of selectable patterns under “Name”. Available types are PRBS, Factory, and User.
Name	Sets the pattern name from the list of patterns filtered by Pat Type.
Pat Invert	Inverts all patterns.
ErRateInjEna	Enables/disables error injection.
ErrInjRate	Sets the error injection rates from 1E-3 to 1E-9.

Label Name	Description
ErrInjSingle	Injects a single error each time the EXEC softkey is pressed.
Deemphasis[1]	
Pre	Adjusts the impulse response sample of the bit before the cursor bit.
Post1	Adjusts the impulse response sample of the first bit after the cursor bit.
Post2	Adjust the impulse response sample of the bit that is two bits after the cursor bit.
Post3	Adjust the impulse response sample of the bit that is three bits after the cursor bit.

[1] Feature available in pattern generator with de-emphasis only.

Refer to Table 20 for the Error Det menu descriptions.

Table 20. Error Det menu descriptions

Label Name	Description
iBER	Displays the instantaneous bit error rate. The iBER is updated at a constant rate, regardless of whether an accumulated BER test is running.
Input Adjust	
SmplV	Sets the sampling voltage that the error detector uses to sample the incoming data. If Set SmplV is on, this value will be updated to the optimal value found during an auto alignment. Resolution is 0.001 V.
Delay	Sets the sampling delay. This sets the amount the clock must be shifted to sample the incoming data to the error detector. In most cases, this value will be centered in the received eye for best performance using the auto alignment feature. If Autoalign parameter - Set Delay is on, this value will be updated to the optimal value found during an auto alignment. Resolution is 0.002 UI.
TermV	Sets the input termination voltage applied to the inputs of the error detector. Resolution is 0.001 V.
DRate	Displays the current data rate.

Label Name	Description
Pattern Menu	
Auto Pattern	Enables/disables the detected pattern selection feature. This feature detects and syncs to PRBS patterns only. When enabled, Pat Type is set to PRBS and cannot be changed.
Pat	Displays the current pattern name (read only). Use the Pat Type and Name menu items to select the desired pattern.
Pat Type	Sets the filter for the list of selectable patterns under “Name”. Available filters are PRBS, Factory, and User. If Auto Pattern is enabled and it cannot determine the pattern type, the message “Unknown” is displayed.
Name	Sets the pattern name from the list of patterns filtered by Pat Type.
Pat Invert	Inverts all patterns. Cannot be changed when Auto Pattern is ON.
Sync Menu	
Sync Now	Executes a synchronization to synchronize to the incoming data stream regardless of the setting for Sync Mode.
Sync Type	Displays the synchronization type (Normal).
Sync Mode	Specifies whether the error detector will attempt to automatically synchronize (Auto) to the incoming data stream or will synchronize only when the Sync Now command is executed (Manual).
Sync Loss / Synchronized	Displays whether the system is synchronized or has lost synchronization.
BER Thrshld	Sets the synchronization threshold to trigger a synchronization attempt. When the Sync Mode is set to Auto and the BER rises above this threshold, the error detector will attempt to synchronize to the incoming data stream automatically. Range is 1E-2 to 1E-9.
AutoAlign Menu	
Perform AutoAlign	Executes an auto alignment to adjust to the optimal sampling and delay voltage.
Config AutoAlign	Set SmplV: enables/disables auto sample voltage alignment. SmplV Step: sets the sampling threshold voltage step size used during an auto alignment to determine the optimal voltage. Set Delay: enables/disables auto delay alignment. Dly Step: sets the sampling delay step size used during an auto alignment to determine the optimal sampling delay.
AutoAlign Results	Eye Height: returns the eye height found during auto alignment. Eye Width: returns the eye width found during auto alignment. Last AutoAlign: returns the date and time of the last auto alignment.

Label Name	Description
Accumulation Menu	
Start Accum	Executes an accumulated BER test.
Stop	Manual: sets the accumulated BER test to run indefinitely (max 9999999.9 seconds ~ 115 days) and is stopped by the user selecting the Stop softkey. Duration: sets the accumulated BER test to run for the duration specified using the Dur setting. Bits: sets the accumulated BER test to run until the number of bits is reached, as specified using the Bit command. Errors: sets the accumulated BER test to run until the number of errors is reached, as specified using the Err command.
Config Stop Menu	Dur: sets the duration of the accumulated BER test in seconds when Duration is selected as the Stop criteria. Maximum is 9999999.9 seconds. Bit: sets the number of bits to accumulate when Bits is selected as the Stop criteria. Range is 1E8 to 1E17 bits. Err: sets the number of errors to accumulate when Errors is selected as the Stop criteria. Range is 1 to 99999999 errors.
Results	aBER: displays the accumulated bit error rate. Selecting the LARGE softkey displays the accumulated BER is a large font. Clear: clears the current results after accumulation is stopped. Errs: displays the number of errored bits. Errored 1: displays the number of logic 1 errors. Errored 0: displays the number of logic 0 errors. Elapsed Time: displays the elapsed time of the BER test.

Refer to Table 21 for the System menu descriptions.

Table 21. System menu descriptions

Label Name	Description
Event Log	Accesses the list of error messages. The Attention LED indicator on the front panel is lit when an error occurs and added to the Error Log.
Save / Recall	Stores the current instrument state into a buffer (1-5), which can then be recalled.
GPIB Address	Sets the GPIB Address from 0 to 30.
Real Time Clock	Sets the instrument time and date.
Instrument Info	Accesses the instrument serial number and firmware version information.
UI Info	Accesses the user interface hardware version and build information.
Controller Info	Accesses the controller hardware version and build information.
Jit Head Info	Accesses the serial number, hardware version, and firmware version information of a pattern generator head that is connected to the Jitter port.
Dly Head Info	Accesses the serial number, hardware version, and firmware version information of a pattern generator or error detector head that is connected to the Delay port.

3.21 Working with Setting Dependencies

The N4960A serial BERT 17 and 32 Gb/s has a number of settings which have a dependency on another setting, noted in the tables above in italic text.

Table 22 contains a summary of all dependent settings. When a conflict between multiple settings is detected, the N4960A serial BERT controller front panel gives the user the opportunity to clear the conflicts in order to proceed with the desired setting.

Table 22. Summary of dependent settings

Settings	Dependency
Clock Source and SSC Enable	SSC cannot be enabled if the clock source is set to external and vice versa.
Offset, Termination (all clock outputs)	On all clock outputs, the range of the offset voltage is defined by the current termination voltage and vice versa. See **Figure 39**.
Offset, Termination, and Coupling (all clock outputs)	On all clock outputs, the coupling must be set to DC in order for the offset and termination voltage to be set to a non-zero value.
PJ vs. all other jitter sources	PJ cannot be enabled if any other jitter source is enabled and vice

Settings	Dependency
	versa.
PJ amplitude vs. PJ frequency	The PJ amplitude range is a function of PJ frequency. The system will resolve conflicts in the PJ amplitude when the PJ frequency is adjusted. However it will simply limit the PJ amplitude range according to the current PJ frequency.
External jitter low band vs. all other jitter sources	External jitter low band cannot be enabled if any other jitter source is enabled and vice versa.
SJ1, SJ2, RJ, external jitter high band	These high frequency band jitters can all be enabled at the same time, however, the sum of their amplitudes must be kept below the specified maximum modulation level.

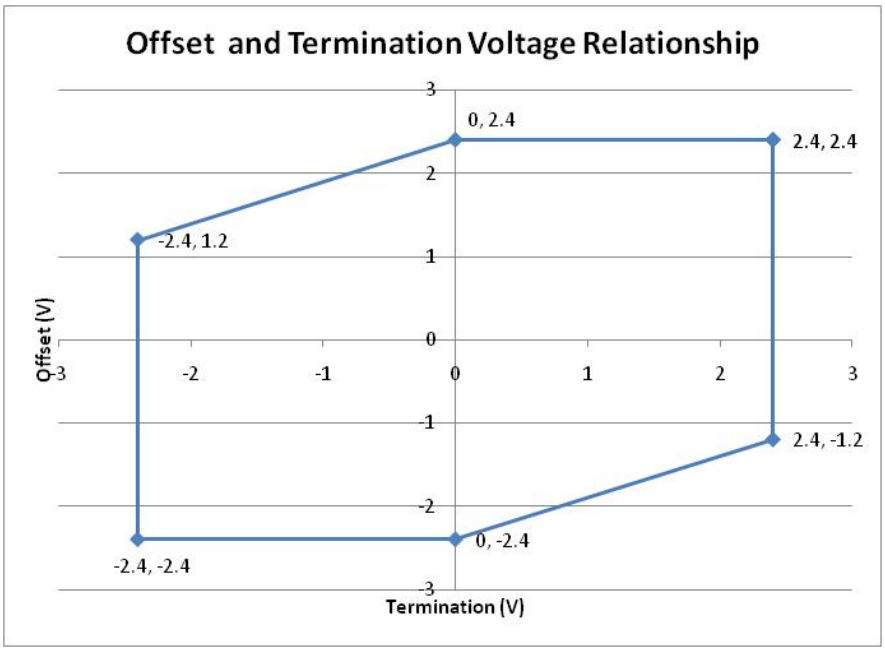


Figure 39. Relationship between offset and termination voltage of the clock outputs

3.22 Verifying Operation

The following procedures will familiarize you with the features of the N4960A Serial BERT 17 and 32 Gb/s and provide a quick check of system operation. The procedures all assume starting from a power up preset state. In all cases where the preset value of the setting parameter can be used, no steps are included to set the value.

3.22.1 Initial Hardware Setup – Controller and Pattern Generator

1. Connect the equipment as shown in Figure 40.
2. Tighten cables to 8 lbf-in (90 N-cm).

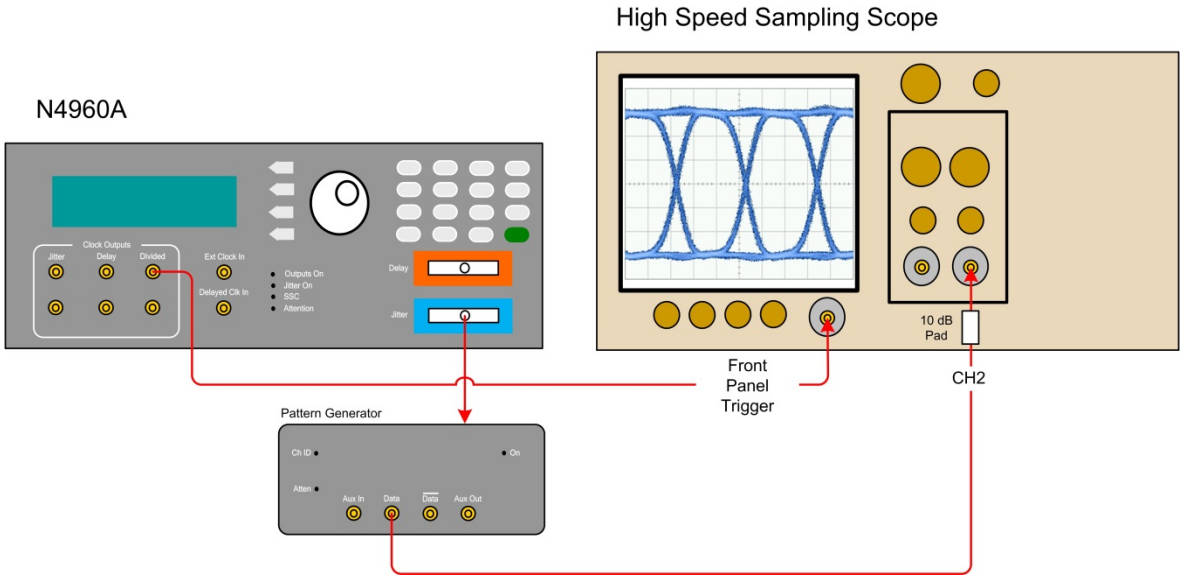


Figure 40. Setup for checking jitter

3.22.2 Initial Settings

1. Set up the high speed sampling scope as follows:

NOTE For purposes of this example setup, an Keysight 86100C Infiniium DCA-J was used. High-speed sampling scope setup option names may differ between models. Signal path delays will be affected by cable lengths. It may be necessary to adjust the scope delay values to center the waveform for proper viewing.

Set the high speed sampling scope to Eye/Mask mode

Trigger Setup

Trigger Level:	0 V
Slope:	Rising Edge
Trigger Bandwidth:	Standard (DC-3.2 GHz)

Timebase Setup

Scale:	20 ps/div
Reference:	center

Channel 2 Setup (data)

Attenuation:	10 dB (10 dB attenuator placed at the input)
Bandwidth:	set to maximum
Display:	On
Scale:	100 mV/Div
Offset:	0.0 V
Units:	Volt

2. Turn the N4960A serial BERT controller on and wait until the MAIN menu appears on the display.
3. In the MAIN menu position the arrow next to the Synthesizer Menu label then press the softkey corresponding to the SEL label.
4. In the Synthesizer Menu position the arrow next to the Frq label then press the softkey corresponding to the EDIT label.
5. Enter 8 on the numeric keypad then press the softkey corresponding to the GHz label to set the frequency to 8 GHz.

NOTE Refer to **3.20.2 Changing Parameters** for instructions on how to use the rotary knob or numeric keypad to make changes.

6. Press the softkey corresponding to the **BACK** label until the **MAIN** menu appears.
7. In the **MAIN** menu position the arrow next to the **Pat Gen-Jit Menu** label then press the softkey corresponding to the **SEL** label.
8. In the **Pat Gen-Jit Menu** position the arrow next to the **Data Output Menu** label then press the softkey corresponding to the **SEL** label.
9. In the **Data Output Menu** position the arrow next to the **Enable** label then press the softkey corresponding to the **EDIT** label.
10. Use the rotary knob to set **Enable** to **ON.** A “clean” eye pattern should now be displayed on the high speed sampling scope similar to the one shown in Figure 41.

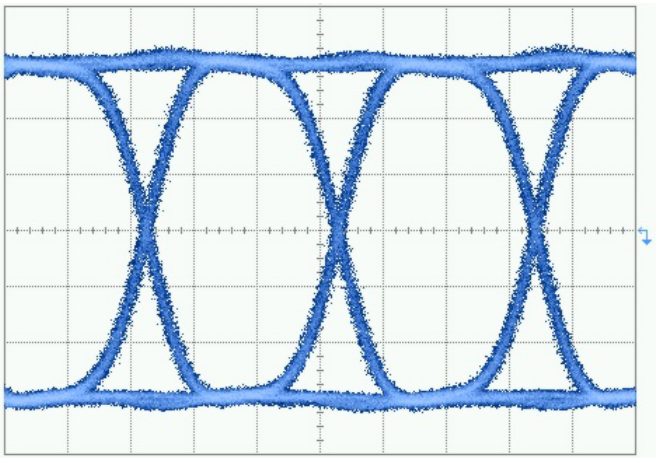


Figure 41. “Clean” eye pattern example

3.22.3 Enabling Sinusoidal Jitter

1. In the **Data Output Menu** position the arrow next to the **SJ1** label then press the softkey corresponding to the **EDIT** label.
2. Enter **200** on the numeric keypad then press the softkey corresponding to the **MHz** label to set the SJ1 level to 200 MHz.
3. In the **Data Output Menu** position the arrow next to the **SJ1Amp** label then press the softkey corresponding to the **EDIT** label.
4. Enter **0.200** on the numeric keypad then press the softkey corresponding to the **UI** label to set the SJ1 modulation to 0.2 UI.
5. In the **Data Output Menu** position the arrow next to the **SJ1Enable** label then press the softkey corresponding to the **EDIT** label.

6. Use the rotary knob to set **SJ1Enable** to **ON**.
7. Press the softkey corresponding to the **SEL** label to accept the entry and return to the **Data Output Menu**. A jittered eye pattern should now be displayed on the high speed sampling scope similar to the one shown in Figure 42.

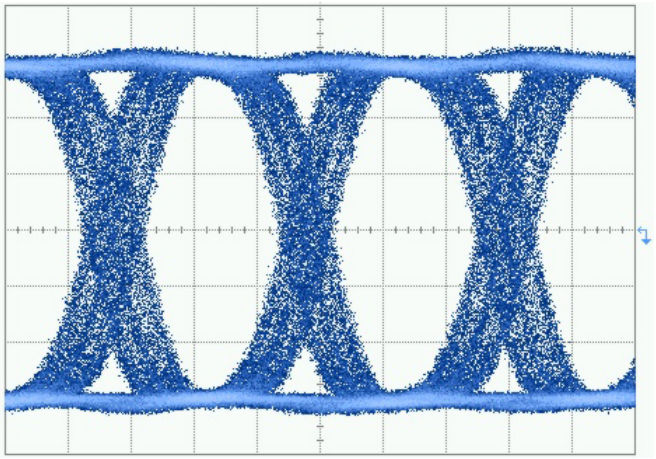


Figure 42. Jittered eye pattern example

8. In the **Data Output Menu** position the arrow next to the **SJ1Enable** label then press the softkey corresponding to the **EDIT** label.
9. Use the rotary knob to set **SJ1Enable** to **OFF**.
10. Press the softkey corresponding to the **SEL** label to accept the entry and return to the **Data Output Menu**.

3.22.4 Enabling Random Jitter (N4960A-CJ1 controller only)

1. In the **Data Output Menu** position the arrow next to the **RJAmp** label then press the softkey corresponding to the **EDIT** label.
2. Enter **050** on the numeric keypad then press the softkey corresponding to the **mUI-rms** label to set the RJ amplitude to 50 mUI-rms.
3. In the **Data Output Menu** position the arrow next to the **RJEnable** label then press the softkey corresponding to the **EDIT** label.
4. Use the rotary knob to set **RJEnable** to **ON**.
5. Press the softkey corresponding to the **SEL** label to accept the entry and return to the **Data Output Menu**. A random jittered eye pattern should now be displayed on the high speed sampling scope similar to the one shown in Figure 43.

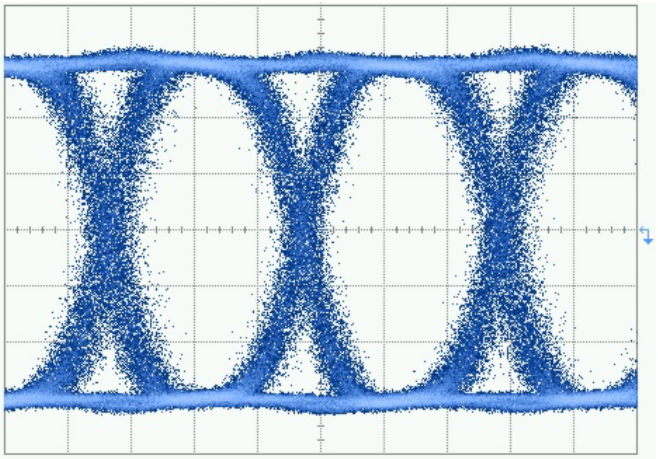


Figure 43. Random jittered eye pattern example

6. In the **Data Output Menu** position the arrow next to the **RJEnable** label then press the softkey corresponding to the **EDIT** label.
7. Use the rotary knob to set **RJEnable** to **OFF**.
8. Press the softkey corresponding to the **SEL** label to accept the entry and return to the **Data Output Menu.**
9. Press the softkey corresponding to the **BACK** label to return to the **MAIN** menu.

3.22.5 Enabling Spread Spectrum Clock (N4960A-CJ1 controller only)

1. In the **MAIN** menu position the arrow next to the **Synthesizer Menu** label then press the softkey corresponding to the **SEL** label.
2. In the **Synthesizer Menu** position the arrow next to the SSCDev label then press the softkey corresponding to the **EDIT** label.
3. Enter **4500** on the numeric keypad then press the softkey corresponding to the **PPM** label to set the spread spectrum to 4500 ppm.
4. In the **Synthesizer Menu** position the arrow next to the **SSCEnable** label then press the softkey corresponding to the **EDIT** label.
5. Use the rotary knob to set **SSCEnable** to **ON**.
6. Press the softkey corresponding to the **SEL** label to accept the entry and return to the **Synthesizer Menu**. A waveform similar to the one shown in Figure 44 should now be displayed on the high speed sampling scope.

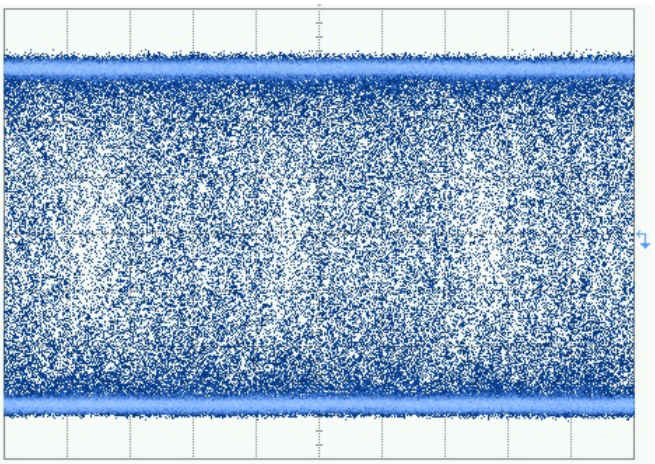


Figure 44. Spread spectrum clock waveform example

7. In the **Synthesizer Menu** position the arrow next to the **SSCEnable** label then press the softkey corresponding to the **EDIT** label.
8. Use the rotary knob to set **SSCEnable** to **OFF**.
9. Press the softkey corresponding to the **SEL** label to accept the entry and return to the **MAIN** menu. Note the waveform displayed on the oscilloscope again shows a clean eye pattern.

3.22.6 Bit Error Rate Test

1. Connect the equipment as shown in Figure 45.
2. Tighten cables to 8 lbf-in (90 N-cm).

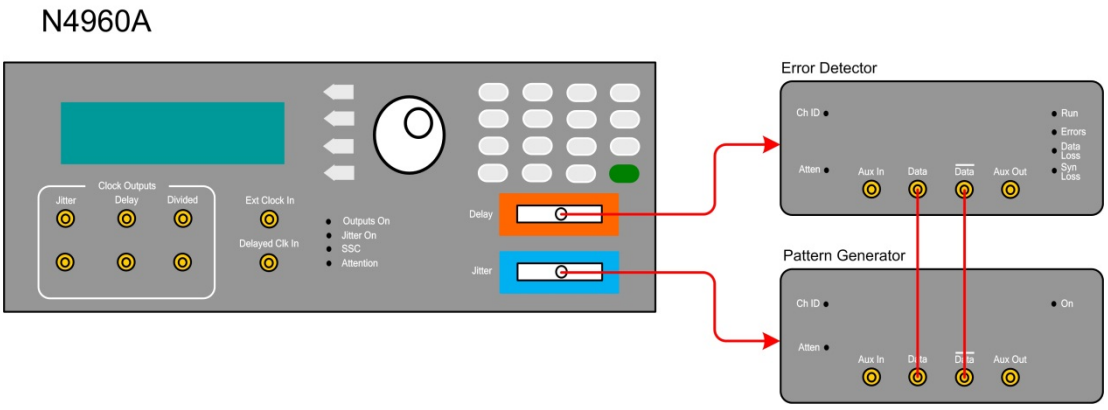


Figure 45. Setup for BER test

3. Ensure that the pattern generator output is enabled. Refer to 3.22.2 Initial Settings for the procedure to enable the pattern generator output.
4. In the MAIN menu position the arrow next to the Err Det Menu label then press the softkey corresponding to the SEL label.
5. In the Err Det Menu position the arrow next to the AutoAlign Menu label then press the softkey corresponding to the SEL label.
6. Position the arrow next to the Perform AutoAlign label then press the softkey corresponding to the EXEC label. A small clock appears in the display. When the clock disappears, ensure that the Errors, Data Loss, and Sync Loss LEDs on the front panel of the error detector are off.
7. Press the softkey corresponding to the BACK label to return to the Err Det Menu.
8. In the Err Det Menu position the arrow next to the Accumulation Menu label then press the softkey corresponding to the SEL label.
9. Position the arrow next to the Stop label then press the softkey corresponding to the EDIT label.
10. Use the rotary knob to set the Stop criteria to Duration.
11. Press the softkey corresponding to the EXIT label to accept the entry.
12. Position the arrow next to the Config Stop Menu label then press the softkey corresponding to the SEL label.
13. Position the arrow next to the Dur label then press the softkey corresponding to the EDIT label.
14. Enter 60 on the numeric keypad then press the softkey corresponding to the SEC label to set the duration to 60 seconds.
15. Press the softkey corresponding to the BACK label to return to the Accumulation Menu.
16. Position the arrow next to the Start Accum label then press the softkey corresponding to the START label. The Run LED on the front panel of the error detector should be lit.
17. When the bit error rate test has completed, position the arrow next to the Results label then press the softkey corresponding to the SEL label.
18. Ensure that Errs reads 0.000e0.

3.23 Setting Frequency and Output Amplitude

The following procedure shows how to set the frequency and clock output amplitude of the N4960A serial BERT controller. The settings are output to either the Jitter or Delay clock connectors on the front panel of the N4960A serial BERT controller.

1. In the MAIN MENU position the arrow next to the Synthesizer Menu label then press the softkey corresponding to the SEL label.
2. In the Synthesizer Menu position the arrow next to the Frq label then press the softkey corresponding to the EDIT label.
3. Adjust the synthesizer frequency using the rotary knob or the numeric keypad.

NOTE Refer to **3.20.2 Changing Parameters** for instructions on how to use the rotary knob or numeric keypad to make changes.

4. Press the softkey corresponding to the EXIT label to accept the entry and return to the MAIN MENU.
5. Determine which clock output will be used. Either the Jitter or Delay output can be used as a "clean" (non-jittered or non-delayed) output provided that the corresponding jitter enable function is set to OFF and the delay is set to 0.
6. In the MAIN MENU position the arrow next to the Jit Clk Out Menu (if using the Jitter clock output) or the Dly Clk Out Menu label (if using the Delay clock output) then press the softkey corresponding to the SEL label.
7. In the Jit Clk Out Menu or the Dly Clk Out Menu position the arrow next to the Amp label then press the softkey corresponding to the EDIT label.
8. Adjust the output amplitude using the rotary knob or the numeric keypad.
9. Press the softkey corresponding to the EXIT label to accept the entry.

3.24 Setting Random Jitter Injection (N4960A-CJ1 controller only)

The following procedure shows how to enable and set the random jitter modulation. The settings are output to the Jitter clock connector on the front panel of the N4960A-CJ1 controller and to a pattern generator connected to the Jitter port.

1. In the MAIN MENU position the arrow next to the Jit Clk Out Menu label then press the softkey corresponding to the SEL label.
2. In the Jit Clk Out Menu position the arrow next to the Amp label then press the softkey corresponding to the EDIT label.
3. Adjust the jittered clock output amplitude using the rotary knob or the numeric keypad.

NOTE Refer to **3.20.2 Changing Parameters** for instructions on how to use the rotary knob or numeric keypad to make changes.

4. Press the softkey corresponding to the EXIT label to accept the entry.
5. Adjust the random jitter modulation using the rotary knob or the numeric keypad.
6. Position the arrow next to the RJEnabl label then press the softkey corresponding to the EDIT label.
7. Use the rotary knob to set RJEnabl to ON.
8. Press the softkey corresponding to the SEL label to accept the entry and return to the MAIN MENU.

3.25 Setting Sinusoidal Jitter Injection

The following procedure shows how to set up a single sinusoidal jitter path. The settings are output to the Jitter clock connector on the front panel of the N4960A serial BERT controller and to a pattern generator connected to the Jitter port.

1. In the Jit Clk Out Menu position the arrow next to the SJ1 label then press the softkey corresponding to the EDIT label.
2. Adjust the SJ1 frequency using the numeric keypad.
3. Position the arrow next to the SJ1Amp label then press the softkey corresponding to the EDIT label.
4. Adjust the SJ1 modulation using the rotary knob or the numeric keypad.
5. Position the arrow next to the SJ1Enabl label then press the softkey corresponding to the EDIT label.

6. Use the rotary knob to set SJ1Enabl to ON.
7. Press the softkey corresponding to the SEL label to accept the entry and return to the MAIN MENU.

3.26 Setting External Jitter High Frequency Injection

The following procedure shows how to set up the external high frequency (low deviation) jitter path. This procedure requires an external jitter source be connected to the Ext Jitter In connector on the rear panel of the N4960A serial BERT controller.

1. In the MAIN MENU position the arrow next to the Jit Clk Out Menu label then press the softkey corresponding to the SEL label.
2. In the Jit Clk Out Menu position the arrow next to the ExtJit label then press the softkey corresponding to the EDIT label.
3. Use the rotary knob to set ExtJit to High Band.
4. Press the softkey corresponding to the SEL label to accept the entry and return to the Jit Clk Out Menu.

NOTE When the high frequency jitter path is enabled, there may be a phase shift in the jittered clock and the pattern generator output. This shift only occurs when SJ1, SJ2, RJ, or ExtHiBand is enabled/disabled. It does not occur when the jitter amplitude or frequency is changed.

3.27 Setting Delay Clock Output

The following procedure shows how to set up the delay clock output. The settings are output to the Delay clock connector on the front panel of the N4960A serial BERT controller.

1. In the MAIN MENU position the arrow next to the Dly Clk Out Menu label then press the softkey corresponding to the SEL label.
2. In the Dly Clk Out Menu position the arrow next to the OutEnabl label then press the softkey corresponding to the EDIT label.
3. Use the rotary knob to set OutEnabl to ON then press the softkey corresponding to the SEL label to accept the entry.
4. In the Dly Clk Out Menu position the arrow next to the Amp label then press the softkey corresponding to the EDIT label.
5. Adjust the delayed clock output amplitude using the rotary knob or the numeric keypad.

NOTE Refer to **3.20.2 Changing Parameters** for instructions on how to use the rotary knob or numeric keypad to make changes.

6. Press the softkey corresponding to the EXIT label to accept the entry.

3.28 Setting Divided Clock Output

The following procedure shows how to set up the divided clock output. The output is taken from the Divided clock output connector on the front panel of the N4960A serial BERT controller.

1. In the MAIN MENU position the arrow next to the Div Clk Out Menu label then press the softkey corresponding to the SEL label.
2. In the Div Clk Out Menu position the arrow next to the OutEnabl label then press the softkey corresponding to the EDIT label.
3. Use the rotary knob to set OutEnabl to ON then press the softkey corresponding to the SEL label to accept the entry.
4. In the Div Clk Out Menu position the arrow next to the Amp label then press the softkey corresponding to the EDIT label.
5. Adjust the divided clock output amplitude using the rotary knob or the numeric keypad.

NOTE Refer to **3.20.2 Changing Parameters** for instructions on how to use the rotary knob or numeric keypad to make changes.

6. Press the softkey corresponding to the EXIT label to accept the entry.

3.29 Event/Error Log

Refer to Table 23 and Table 24 for the list of message origins and values found in the event/error Log.

NOTE When an event/error is received, the Attention LED will illuminate.

Each event log entry contains the following information:

- Log Number: 1 to n, with 1 being the most recent error and 'n' being the oldest error.
- Message Origin: Identifies the sub-system which produced the error.
- Message Value: The error.
- Datestamp: Date of error receipt (mm/dd/yy).
- Timestamp: Time of error receipt (hh/mm/ss).

Table 23. Message origin

Message Origin	Description
IPC	IPC protocol related codes
FREQ	Frequency control
PHASE	Phase control
REF	10 MHz reference clock

Table 24. Message values

Message Values	Description
OK	Status good, no errors
UNK	Status unknown
ERR	Misc. error
LOS	Loss of signal/phase slip
OOR	Value out of range
TIMEOUT	Command or operation took too long. See Section 6.17.4.
AMPL_LIMIT_WARN	Amplitude limited, non-fatal (warning), used for PJ amplitude adjustment during SCPI PJ frequency setting. See Section **6.10.1**.
INTERNAL	Used to indicate the 10MHz reference clock is set to Internal
EXTERNAL	Used to indicate the 10MHz reference clock is set to External

4 Applications

4.1 Introduction

The N4960A serial BERT 17 and 32 Gb/s performs basic BER and jitter tolerance testing or general receiver characterization applications.

In a general BERT application, the outputs would be configured as follows:

Jitter connector is used to drive the pattern generator. Stress can be applied for jitter tolerance testing or other receiver characterization testing.

Delay connector is used to clock the error detector. The delay feature enables the detector to synchronize with the pattern, and align to sample at the center of the eye (optimum decision point).

Divided Output can provide a sub rate of the clock to trigger a sampling oscilloscope. Most sampling scopes have maximum trigger rates which are substantially lower than the bandwidth of the sampler. When used in high data rate applications, the data clock must be divided down to a ratio within the maximum trigger rate. In addition, by setting the divider ratio to the exact pattern length, the output will be locked to the pattern. Using this signal to trigger the sampling scope allows the user to view and measure the actual bit stream, rather than presenting an “eye” of overlaid bits.

The divided output can also be used where a sub rate clock is required.

4.2 Testing Transceivers Used in Fibre Channel Networks

There are three topologies in this type of network including point-to-point, arbitrated loop, and switched fabric. The connections between devices use transceivers for optimization. For example, in a switched fabric topology, SFP+ (8GFC and 16GFC), XFP (10 Gb/s) and SFP (≤ 4 Gb/s) are types of transceivers that connect between the switched fabric and various devices such as storage and computing equipment. Typical patterns used to test transceiver devices include PRBS series, JSPAT, and K28 series which are part of the preloaded library of patterns in the N4960A 32G BERT.

For 16GFC applications (14.025 Gb/s), the N4960A can perform BER measurements and can provide a stressed pattern generator signal for receiver tests. The N4960A, used with the N4980A multi-instrument BERT software, can also provide jitter tolerance tests for accurate characterization.

1. Turn the N4960A serial BERT controller on and wait until the MAIN menu appears on the display.
2. In the MAIN menu position the arrow next to the Synthesizer Menu label then press the softkey corresponding to the SEL label.
3. In the Synthesizer Menu position the arrow next to the Frq label then press the softkey corresponding to the EDIT label.
4. Enter the frequency using the numeric keypad then press the softkey corresponding to the GHz label. The data rate is double the synthesizer frequency and is based on the type of transceiver being tested.
5. Press the softkey corresponding to the BACK label until the MAIN menu appears.
6. In the MAIN menu position the arrow next to the Pat Gen Menu label then press the softkey corresponding to the SEL label.
7. In the Pattern Gen Menu position the arrow next to the Data Output Menu label then press the softkey corresponding to the SEL label.
8. In the Data Output Menu position the arrow next to the Enable label then press the softkey corresponding to the EDIT label.
9. Use the rotary knob to set Enable to ON.
10. Press the softkey corresponding to the EXIT label to accept the entry and return to the Data Output Menu.
11. Press the softkey corresponding to the BACK label to return to the Pattern Gen Menu.
12. In the Pattern Gen Menu position the arrow next to the Pattern Menu label then press the softkey corresponding to the SEL label.

13. Position the arrow next to the Name label then press the softkey corresponding to the SEL Label.
14. Select the pattern based on the type of transceiver being tested.
15. Press the softkey corresponding to the BACK label until the MAIN menu appears.
16. In the MAIN menu position the arrow next to the Err Det Menu label then press the softkey corresponding to the SEL label.
17. In the Err Det Menu position the arrow next to the AutoAlign Menu label then press the softkey corresponding to the SEL label.
18. Position the arrow next to the Perform AutoAlign label then press the softkey corresponding to the EXEC label. A small clock appears in the display. When the clock disappears, ensure that the Errors and Data Loss LEDs on the front panel of the error detector are off.
19. Press the softkey corresponding to the BACK label to return to the Err Det Menu.
20. In the Err Det Menu position the arrow next to the Accumulation Menu label then press the softkey corresponding to the SEL label.
21. Position the arrow next to the Start Accum label then press the softkey corresponding to the START label. The Run LED on the front panel of the error detector should be lit.
22. To stop the BER measurement, press the softkey corresponding to the STOP label.
23. Position the arrow next to the Results label then press the softkey corresponding to the SEL label.
24. View accumulated BER (aBER), total errors (Errs), one errors (Errored 1), zero errors (Errored 0), and measurement time (Elapsed Time).

5 Performance Specifications

Specifications describe the instrument's warranted performance. Non-warranted values are stated as typical. All specifications are valid in a range from 15 °C to 35 °C ambient temperatures after a 30-minute warm-up phase. Unless stated otherwise, all specifications are valid at the output connectors.

5.1 N4960A Clock Source/BERT Controller Non-stressed Specifications

Table 25 shows the N4960A clock source/BERT controller specifications (non-stressed features).

Table 25. N4960A clock source/BERT controller non-stressed specifications

Parameter	Specification
Configuration	Frequency synthesizer with three differential outputs: Jitter, Delay, and Divided. Clock generator Jitter and Delay clocks are shared with the remote head port connectors. Changing the controller clock output parameters while pattern generator and/or error detector remote heads are operating will effect their operation. Pattern generator and error detector remote heads operate with a half-rate clock - therefore the remote head Data rate will be double the frequency of the controller Clock.
Frequency	1 to 16 GHz with no remote heads connected 2 to 8.5 GHz when one or two 17 Gb/s remote heads are connected 2 to 16 GHz when one or two 32 Gb/s remote heads are connected
Frequency Resolution	1 kHz (front panel)
Outputs	Jitter (stressed), Delay, and Divided (non-stressed)
Output Configuration	
All Outputs	Differential, with amplitude, offset, and termination voltage adjustment (can be used single ended without terminating unused outputs)
Amplitude Range	300 mV to 1.7 V (p-p), single ended

Parameter	Specification
Offset Range	–2.4 V to +2.4 V, limited by termination voltage. See **Figure 39**. On divided clock output, this is only valid when the divide ratio is a power of 2.
Termination Voltage Range	–2.4 V to +2.4 V, limited by offset voltage. See **Figure 39**.
Rise Time (20% - 80%)	< 23 ps
Intrinsic Jitter	< 700 fs rms typical from 2 to 16 GHz
Duty Cycle	
Jitter and Delay Outputs	50% ±5%
Divided Output	50% ±5% at divide ratios which are a power of 2. Duty cycle varies between 33 and 66% at divide ratios which are not a power of 2. 50% ±10% when divide ratio is set to 1 for amplitudes ≥500 mV.
Frequency Accuracy	±1 ppm typical, ±5 ppm maximum
Reference Frequency	10.0 MHz, single ended output and input on rear panel
External Clock	Single ended input can be substituted for internal synthesizer, drives all clocks
Maximum clock input amplitude	2 V (p-p)
Clock input sensitivity	200 mV typical
External Delayed Clock Input	Single ended input drives Delay clock outputs only Maximum delayed clock input amplitude 2 V (p-p) Delayed clock input sensitivity 150 mV typical
Spread Spectrum Clock (N4960A-CJ1 only)	Phase deviation appears on all outputs (internal synthesizer only)
Deviation Range	0% to 1% (10,000 ppm)
Modulation Frequency Range	1 Hz to 50 kHz
Modulation Waveshape	Triangle
Deviation Direction	Down spread, Center spread, or Up spread
Divided Clock Divide Ratio	÷ 1, 2, 3,... 99,999,999, with no missing integers (Waveshape of divided clock slower than ≈ 1 MHz will be differentiated)
Delayed Clock Delay Range	0 to ±1,000 UI
Delayed Clock Delay Resolution	1 mUI
Connector Type	
All signals except 10 MHz Ref In/Out	SMA
10 MHz Ref In, Out	BNC

5.2 N4960A Clock Source/BERT Controller Jitter Specifications

Table 26 shows the N4960A clock source/BERT controller jitter specifications.

Table 26. N4960A clock source/BERT controller jitter specifications

Parameter	Specification
Configuration	Calibrated stress is added to Jitter Clock Output and the Jitter remote head port clock through one of two modulators: a high deviation, low frequency path, or a low deviation, high frequency path. The amplitude of any stress appearing on the front panel Jitter Clock Output will be 1/2 of the value appearing at the N4951A/B remote head pattern generator Data output (if connected to the Jitter port). Changing stress amplitudes on the front panel Jitter Clock Output will also change the level appearing on the pattern generator Data output (connected to the Jitter port).
Options	
N4960-CJ0	Single tone sinusoidal jitter, low (SJ) and high (PJ) deviation, plus external input
N4960-CJ1	Two internal sinusoidal jitter, true random (RJ) jitter, plus external input
SJ Frequency Range	With no pattern generator head connected to jitter port: 1 Hz to 200 MHz With an N4951A/B pattern generator head connected to Jitter port: 1 Hz to 150 MHz, over-programmable to 200 MHz

Parameter	Specification
SJ modulation range With no pattern generator head connected to the Jitter port: Front panel output frequency 1 to 3 GHz > 3 to 16 GHz With an N4951A/B pattern generator head connected to the Jitter port: Front panel output frequency > 2 to 16 GHz	Range of SJ1 and SJ2. The maximum combined peak jitter of SJ1 + SJ2 + RJ (p-p) + external jitter are applied to the high frequency band modulator (see **Figure 46**, **Figure 47**, **Figure 48**). 0 to 1.0 UI p-p for modulation frequency 1 Hz to 100 MHz, 0 to 0.5 UI p-p for modulation frequency > 100 MHz to 200 MHz, over-programmable to 1.0 UI 0 to 1.0 UI p-p for modulation frequency 1 Hz to 100 MHz, 0 to 0.7 UI p-p for modulation frequency > 100 MHz to 200 MHz, over-programmable to 1.0 UI 0 to 0.4 UI p-p for modulation frequency 1 Hz to 30 MHz, 4 to 32 Gb/s 0 to 0.165 UI p-p for modulation frequency > 30 MHz to 150 MHz, 4 to 29 Gb/s 0 to 0.1 UI p-p for modulation frequency > 30 MHz to 150 MHz, >29 to 31.5 Gb/s Over-programmable to 0.5 UI
RJ Modulation Frequency Contour	Flat from DC to modulator band pass: -3 dB at 320 MHz, single pole roll off to 500 MHz. Loop through allows user to customize contour by inserting HPF or LPF in loop on rear panel. Nominal impedance is 50 Ω. Filter insertion loss will lower RJ modulation depth below its calibrated value.
RJ Modulation Range With no pattern generator head connected to the Jitter port:	0 to 25 mUI rms, can be set up to 150 mUI rms, to allow for insertion loss in external filters, but is uncalibrated for settings > 25 mUI. Peak sum of all SJ, RJ and External input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or **Figure 46**, **Figure 47**, **Figure 48**.
RJ Modulation Range with an N4951A/B pattern generator head connected to the Jitter port:	0 to 12 mUI rms, 4 to 29 Gb/s 0 to 7 mUI rms, >29 to 31.5 Gb/s Over-programmable to 25 mUI
RJ Crest Factor	14 minimum (p-p to rms ratio)

Parameter	Specification
External High Frequency Band Input	
Configuration	Wide band low deviation external modulation input. External input is summed with SJ1, SJ2, and RJ. High Frequency Band stress is not available when either Low Frequency PJ or External is selected.
Modulation Frequency Range	DC to at least 350 MHz, determined by high frequency modulator. -3 dB BW ≈ 320 MHz
Modulation Range	Peak sum of SJ and External input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or **Figure 46**, **Figure 47**, **Figure 48**.
Low Frequency (High Deviation) Modulation Configuration	Periodic Jitter (PJ) or External input. SJ and high frequency external modulation sources are not available when either low frequency source is enabled.
Low Frequency Modulation Frequency Range	
PJ	1 Hz to 17 MHz
External	1 Hz to 4 MHz
Low Frequency PJ Modulation Range with no pattern generator head connected to the Jitter port:	
Front panel output frequency > 1 to 16 GHz	0.001 to 100 UI for frequency ≤62.5 kHz 0.001 to (6.25E6/ PJ Frequency) for frequency >62.5 kHz to 17 MHz (see **Figure 46**)
With an N4951A/B pattern generator head connected to the Jitter port:	
Front panel output frequency > 2 to 16 GHz	0.001 to 50 UI for frequency ≤62.5 kHz 0.001 to (3.125E6/ PJ Frequency) for frequency >62.5 kHz to 17 MHz (see **Figure 46**, **Figure 47**, **Figure 48**)

Parameter	Specification
Low Frequency External Modulation Range with no pattern generator head connected to the Jitter port:	
Front panel output frequency > 1 to 16 GHz	0.001 to 50 UI for frequency ≤68.4 kHz 0.001 to (3.42E6/ Modulation Frequency) for frequency > 68.4 kHz to 4 MHz (see **Figure 46**)
With an N4951A/B pattern generator head connected to the Jitter port:	
Front panel output frequency > 2 to 16 GHz	0.001 to 25 UI for frequency ≤68.4 kHz 0.001 to (1.71E6/ Modulation Frequency) for frequency > 68.4 kHz to 4 MHz (see **Figure 46**, **Figure 47**, **Figure 48**)

5.2.1 Maximum N4960A Clock Modulation Range without PG Connected

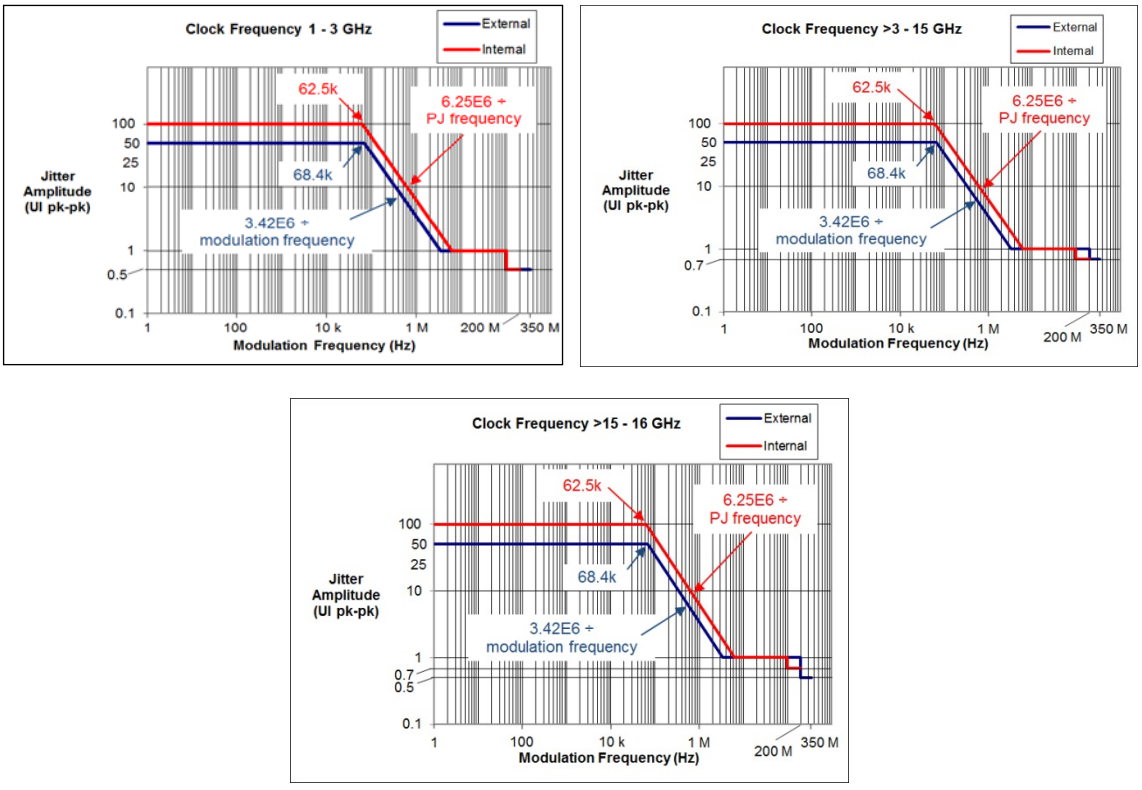


Figure 46. Maximum N4960A JITTER CLOCK OUTPUT modulation amplitude when no remote pattern generator head is attached to the Jitter port

5.2.2 Maximum N4960A Clock Modulation Range with PG Connected

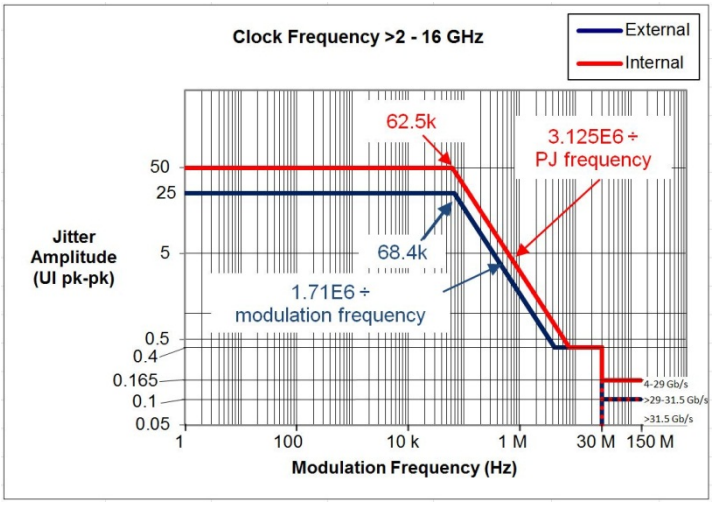


Figure 47. Maximum N4960A JITTER CLOCK OUTPUT modulation amplitude when a remote pattern generator head is attached to the Jitter port

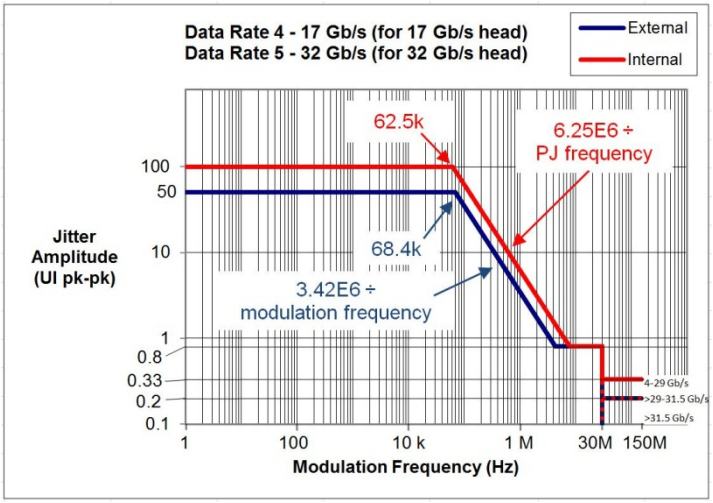


Figure 48. Maximum N4951A/B Pattern Generator Remote Head DATA OUTPUT modulation amplitude

5.3 N4951A/N4951B[7] Pattern Generator Specifications

Table 27 shows the N4951A/N4951B pattern generator specifications.

Table 27. N4951A/N4951B pattern generator specifications

Parameter	Specification
Configuration	Remote mountable head operates with N4960-CJ0/N4960-CJ1.
Data Rate Range	
N4951A-P32/N4951B-H32/ N4951B-D32	5 to 32 Gb/s
N4951A-P17/N4951B-H17/ N4951B-D17	4 to 17 Gb/s
Data Rate Resolution	2 kb/s
Pattern Selection	
PRBS (hardware generated)	$2^n - 1$, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51
Telecom/Datacom	K28.3, K28.5, K28.7, CJPAT, CJTPAT, CRPAT, JSPAT, JTSPAT
Clock	÷2, ÷4, ÷8,..., ÷64. ÷2 = 0101, ÷4 = 0011,..., ÷64 = 32 0's followed by 32 1's
User	1 bit to 8 Mb.
Pattern Invert	Available for all patterns
Error Injection	Single or uniform rate
Error Injection Rates	10^{-n}, n = 3, 4, 5, 6, 7, 8, 9
Output Configuration	Differential. May be operated single end without unused output terminated into 50 Ω. AC Coupled with internal bias tee.
Output Data Connectors	N4951A 2.92 mm female N4951B 2.4 mm female
Output Data Amplitude	
N4951A-P17/N4951A-P32	100 mV (p-p) to 1.0 V (p-p), single ended, in 5 mV steps
N4951B-H17/N4951B-H32	300 mV (p-p) to 3.0 V (p-p), single ended, in 5 mV steps
N4951B-D17/N4951B-D32	300 mV (p-p) to 1.5 V (p-p), single ended, in 5 mV steps
Offset Voltage Range	–2 V to +2 V. Offset range limited by termination voltage
Termination Voltage Range	–2 V to +2 V. Termination voltage limited by Offset Voltage
Output Data Delay Range	0 to ±2,000 UI[6], in 2 mUI steps
Rise Time (20% - 80%)	
N4951A-P17	17 ps typical, 20 ps maximum[1, 3]
N4951A-P32	16 ps typical, 20 ps maximum[2, 3]
N4951B-D17	12 ps typical, 15 ps maximum[1, 4]
N4951B-D32	12 ps typical, 15 ps maximum[2, 4]
N4951B-H17	16 ps typical, 20 ps maximum[1]
N4951B-H32	15 ps typical, 19 ps maximum[2]

Parameter	Specification	
Jitter[6]		
N4951A	1.3 ps rms typical[5]	
N4951B-D17	< 750 fs typical[1, 4, 5]	
N4951B-D32	< 650 fs typical[2, 4, 5]	
N4951B-H17	< 600 fs typical[1, 5]	
N4951B-H32	< 650 fs typical[2, 5]	
De-emphasis configuration	5-tap: pre-cursor, post-cursor 1, post-cursor 2, post-cursor 3	
N4951B-D17	Pre-cursor	0 to +30 dB[8]
N4951B-D32 only	Post-cursor 1	0 to –30 dB[8]
	Post-cursor 2	–30 to +30 dB[8]
	Post-cursor 3	–30 to +30 dB[8]

[1] At 14 Gb/

[2] At 28 Gb/s

[3] At 1 V (p-p) amplitude, single ended

[4] At >= 1 V (p-p) amplitude, single ended

[5] Jitter rms is measured on an eye diagram from 86100 DCA with 70 GHz remote heads and precision time base, N4960A driven with an external clock, for example Keysight E8257D

[6] Data Delay spec applies only to a pattern generator connected to the Delay port

[7] N4951B pattern generator heads are only supported on Keysight N4960A controllers with serial numbers higher than US53083001, otherwise an N4960A controller upgrade is required

[8] Cursor amplitudes are specified relative to the preceding cursor; for example, post-cursor 1 amplitude is relative to the main cursor amplitude; post-cursor 2 amplitude is relative to post-cursor 1; post-cursor 3 amplitude is relative to post-cursor 2; pre-cursor amplitude is relative to post-cursor 3

Parameter	Specification
SJ[1] Frequency Range	1 Hz to 150 MHz, over-programmable to 200 MHz
SJ Modulation Range	Range of SJ1 and SJ2. The maximum combined peak jitter of SJ1 + SJ2 +RJ (p-p) + external jitter are applied to the high frequency band modulator (see **Figure 48**). 0 to 0.8 UI p-p for modulation frequency 1 Hz to 30 MHz, 4 to 32 Gb/s 0 to 0.33 UI p-p for modulation frequency >30 MHz to 150 MHz, 4 to 29 Gb/s 0 to 0.2 UI p-p for modulation frequency >30 MHz to 150 MHz, >29 to 31.5 Gb/s Over-programmable to 1.0 UI
RJ[1] Modulation Range	0 to 24 mUI rms, 4 to 29 Gb/s 0 to 14 mUI rms, >29 to 31.5 Gb/s Over-programmable to 50 mUI rms
Low Frequency PJ[1] Modulation Range	0.002 to 100 UI for frequency ≤ 62.5 kHz 0.002 to (6.26E6 / PJ frequency) for frequency > 62.5 kHz to 17 MHz See **Figure 48**.
Low Frequency External Modulation Range	0.001 to 50 UI for frequency ≤ 68.4 kHz 0.001 to (3.42E6 / modulation frequency) for frequency > 68.4 kHz to 4 MHz See **Figure 48**.
High Frequency External Modulation Range	See **Figure 48**.
Indicators	Ch ID – connected to N4960A channel Atten – error condition occurred and logged in Error Log On – data output on

[1] Jitter injection specifications (SJ, PJ, RJ, Ext) apply only to a pattern generator connected to the Jitter port.

5.4 N4952A-E17/N4952A-E32 Error Detector Specifications

Table 28 shows the N4952A-E17/N4952A-E32 error detector specifications.

Table 28. N4952A-E17/N4952A-E32 error detector specifications

Parameter	Specification
Configuration	Remote mountable head operates with N4960-CJ0/N4960-CJ1.
Data Rate Range	
N4952A-E32	5 to 32 Gb/s
N4952A-E17	4 to 17 Gb/s
Data Rate Resolution	2 kb/s
Pattern selection	
PRBS (hardware generated)	$2^n - 1$, n = 7, 9, 10, 11, 15, 23, 29, 31, 33, 35, 39, 41, 45, 47, 49, 51
Telecom/Datacom	K28.3, K28.5, K28.7, CJPAT, CJTPAT, CRPAT, JSPAT, JTSPAT
Clock	÷2, ÷4, ÷8,..., ÷64. ÷2 = 0101, ÷4 = 0011,..., ÷64 = 32 0's followed by 32 1's
User	1 bit to 8 Mb.
Input Configuration	Differential. May be single end with unused input terminated into 50 Ω. (Termination included) AC Coupled with internal bias tee.
Input Connectors	2.92 mm female
Maximum Input Amplitude	1 V (p-p) single ended; 2 V (p-p) differential
Input Sensitivity	< 85 mV (p-p) single ended[1] (typically <50 mV)
Termination Voltage	–2 V to +2 V
Input Data Delay Range	0 to ±2,000 UI in 2 mUI steps
Input Data Decision Threshold Range	–1 V to +1 V in 1 mV steps
Indicators	Ch ID – connected to N4960A channel Run – BER measurement running Errors – bit errors occurring Data Loss – no data detected Sync Loss – not synchronized to the incoming data stream Atten – error condition occurred and recorded into Error Log

[1] At ≤ 28 Gb/s.

6 Remote Operation

The N4960A serial BERT controller can be controlled and queried with the rear-panel GPIB or USB interface.

6.1 GPIB Interface

The GPIB interface complies with IEEE standard 488.2-1992. To learn more about the GPIB interface, consult the following books from the IEEE:

- The International Institute of Electrical and Electronic Engineers. IEEE Standard 488.1-1987, IEEE Standard Digital Interface for Programmable Instrumentation. New York, NY, 1987.
- The International Institute of Electrical and Electronic Engineers. IEEE Standard 488.2-1987, IEEE Stand Codes, Formats, Protocols and Communication Commands for Use with ANSI/IEEE Std 488.1-1987. New York, NY, 1987.

A GPIB interface requires that all devices on a common bus have different addresses. The address of the N4960A serial BERT 17 and 32 Gb/s is set up using the System Settings menu. The range is 0 to 30.

The GPIB interface capabilities are described in Table 29.

Table 29. N4960A GPIB capabilities

Mnemonic	Function
SH1	Complete source handshake capability
AH1	Complete acceptor handshake capability
T6	Basic talker; serial poll; unaddressed to talk if addressed to listen; no talk only
L4	Basic listener; unaddressed to listen if addressed to talk; no listen only
SR1	Complete service request capability
RL2	Remote/local capability with local lockout (LLO)
PP0	No parallel poll capability
DC1	Device clear capability
DT1	Device trigger capability (accepted but ignored)
C0	No controller capability
E2	Tristate outputs (except the handshake line)

6.2 USB Interface

The USB interface connects to an external PC controller to control the N4960A serial BERT 17 and 32 Gb/s. The USB interface allows the N4960A serial BERT controller to be connected and disconnected without rebooting the computer or turning off the N4960A serial BERT controller (hot swapping).

Connect a Type-A to Type-B 5 pin cable from the USB port of the PC controller to the USB port on the rear panel of the N4960A serial BERT controller.

6.2.1 USB Driver

Installation of the appropriate driver is required. The N4960A serial BERT controller USB port can be accessed from a PC as a virtual COM port (VCP). Virtual COM port drivers cause the USB device to appear as an additional COM port available to the PC. Application software can access the USB device in the same way as it would access a standard COM port.

The appropriate driver for several versions of Microsoft Windows® operating systems is included on a CD-ROM which is shipped with the instrument.

The N4960A serial BERT controller uses a hardware interface IC manufactured by Future Technologies Devices International (FTDI). VCP drivers are available for several operating systems at their web site: www.ftdichip.com/FTDrivers.htm.

6.2.2 USB Programming Note

The FTDI chip, which enables serial port communication over a USB connection, boots at power-on, or preset, with the setting Local Echo = ON. The function returns a text string of each command sent over USB. It is recommended to set the Local Echo = OFF prior to sending any remote commands over USB. The command syntax to turn Local Echo OFF for the FTDI chip is:

!ECHO OFF

Progamming example:

```
# connect to N4972A-CJ0 and turn off local echo if using USB
# -address is "GPIB::18" for GPIB, "ASRL15" for COM15 (USB)
# -local echo may be on or off, which means the !ECHO OFF
#   command may be repeated back to us, this is tricky
print "connecting to " + address
scs = visa.instrument(address)
scs.clear
if (address.find("ASRL") != -1):
   scs.write("!ECHO OFF")
   scs.timeout = 1
   try:
      tmp = scs.read()
   except:
      scs.clear
   scs.timeout = timeout
```

6.3 Remote Command Syntax

The commands and queries are documented in the Backus-Naur Form notation, detailed in Table 30.

Table 30. Remote command and query syntax

Symbol	Meaning
<>	Defined element (for example: <arg>)
::=	Is defined as (for example: <arg> ::= argument)
|	Exclusive OR
{ }	One of this group is required
[ ]	Optional item
...	Previous elements may be repeated

6.3.1 Command Structure

The GPIB and USB interfaces allow commands that tell the instrument to take a specific action. In addition, these interfaces allow queries, which ask the instrument to return information.

Commands are composed of syntactic elements:

- Header – the command name; if it ends with a question mark, it's a query.
- Delimiter – a space ' ', colon ':', comma ',', or semi-colon ';'.
- Link – a command sub-function. Not all commands have links.
- Argument – a quantity, quality, or limit associated with the header or link.

Commands are case insensitive, although they are documented in an uppercase and lowercase manner that indicates the minimum characters required to make the command. The commands can be shortened to the minimum length illustrated by the uppercase letters in the documentation.

- The command
  - :SOURce:FREQuency
- Can be written in lowercase
  - :source:frequency
- And it can be shortened
  - :SOUR:FREQ

6.4 IEEE Common Commands

The IEEE 488.2 standard has a list of reserved commands that must be implemented by all instruments using the standard. The N4960A serial BERT controller implements all of the required commands, listed in Table 31.

Table 31. IEEE common commands

Command	Function
*CLS	Clear status
*ESE	Event Status Enable Register Set
*ESE?	Event Status Enable Register Query
*ESR?	Event Status Register Query
*IDN?	Identification Query
*OPC	Operation Complete clear flag
*OPC?	Operation Complete Query
*RST	Reset
*SRE	Service Request Enable Set
*SRE?	Service Request Enable Query
*STB?	Status Byte Query
*TST?	Self Test Query
*WAI	Wait to continue
IEEE optional commands	
*RCL	Recall
*SAV	Save

6.5 SCPI Mandated Commands

The N4960A serial BERT controller also conforms to the Standard Commands for Programmable Instrumentation (SCPI 1999.0) command set. The SCPI mandated commands that are implemented are listed in Table 32.

Table 32. SCPI mandated commands

Command	Function
:SYSTem:ERRor	Returns the oldest event/error number and message from error queue and removes it.
:SYSTem:VERSion	Returns SCPI protocol version number (“1999.0”)
:SYSTem:ERRor:ALL	Returns all events/error log reports
:SYSTem:COUNt	Returns the number of errors in the queue.

6.6 SCPI Protocol Description

The N4960A serial BERT controller supports a simple SCPI syntax. SCPI has an associated hierarchy with it. The top level is referred to as the Root mode. SCPI remembers the current hierarchy so you do not need to repeat it for subsequent commands.

6.6.1 SCPI Example

The capital letters in the commands denote the required subset of mnemonic for correct state control. The lower case letters are optional but if they are used they must be spelled correctly.

:OUTJitter:AMPLitude?
(Query output jitter amplitude value.)

:OUTJitter:AMPLitude 500mV
(Set output jitter amplitude value.)

AMPLitude?
(Query output jitter amplitude value. Only the AMPLitude? command is required since it is part of the OUTJitter group.)

TERMination 135mV
(Set the termination voltage to 135 mV. Only the TERMination command is required since it is part of the OUTJitter group.)

6.7 SCPI Numeric Parameters and Optional Units

The following are examples of SCPI numeric parameters for SCPI commands that have numeric values:

.2	digits before decimal point not required
500.	digits after decimal point not required
500	no decimal point required
-1000	accepts negative '–' or positive '+' signs
200E-3	accepts uppercase 'E' or lowercase 'e' to specify exponent

The following are examples of optional units:

200 mV	mV used in place of e-3
5MHz	MHz used in place of e6
-1000UI	unit interval of negative 1000.

6.8 Pattern Generator Channelization

Pattern generators can be connected to the jitter or delay connectors on the front panel of the N4960A controller. You can also connect a pattern generator to the jitter connector and another pattern generator to the delay connector for dual pattern generation. Error detectors can only be connected to the delay connector.

In order to send commands to the intended pattern generator, [(@<channel list>)] defines which channel(s) to apply the command. Channel 0 is the jitter channel and channel 1 is the delay channel as shown in Figure 49.

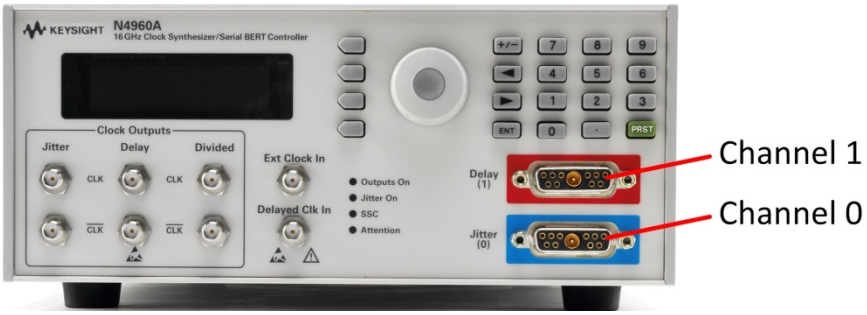


Figure 49. Pattern generator channelization

For example, if two pattern generators are connected, sending the :PG:DATA:OUTPut ON (@ 0:1) command turns on the pattern generator output connected to both channel 0 and channel 1. Channelization applies to the use of pattern generators only.

The channel list is defined within parentheses and always begins with the '@' character followed by either a comma separated set of channels or colon separated channel range. Refer to the following examples:

None affects channel 0 only
(@ 1) affects channel 1 only
(@ 0, 1) affects channels 0 and 1
(@ 0:1) affects channels 0 and 1
(@) affects previously defined channel list

If no channel list is specified, then the command applies to the default channel. The default channel is the jitter channel (channel 0).

Results to queries are always returned in ascending order (channel 0 first, channel 1 last), regardless of the order in the request.

When sending commands to one or more channels, a verification check is performed to ensure that the command and the type of channel match. For queries, if the types do not match, a "?" is returned to indicate a mismatch.

For commands that set parameters, if there is a mismatch in one or more of the remote heads in the channel list, then error code -221, "Settings Conflict" is returned and no action is taken on the command.

6.9 Command Conventions

The following conventions are used in the following summary:

SOURce indicates that the SOUR characters are required and that the keyword may optionally appear as SOURCE instead. No other spellings are valid.

value is a placeholder in the command and is described elsewhere in the text for the command.

[unit] indicates that the unit placeholder is optional; it may or may not appear in the command.

string is a placeholder in the command and is described elsewhere in the text for the command.

ON | OFF indicates a choice may be made between ON or OFF.

{ ON | OFF } indicates that a choice *must* be made between ON or OFF; one or the other must appear in the command.

6.10 SCPI Standard Negative Event/Error Codes

The following table represents the SCPI standard event/errors used by the N4960A serial BERT controller.

Table 33. SCPI standard negative event/error codes

Error/Event Code	Description
0, “No error”	Event/error queue is empty.
-100, “Command error”	Indicates that an undefined command was received via the SCPI interface.
-102, “Syntax error”	An unrecognized command or data type was encountered.
-103, “Invalid separator”	The parser was expecting a separator and encountered an illegal character.
-109, “Missing parameter”	Fewer parameters were received than required for the header.
-221, “Settings conflict”	A legal program data element was parsed but could not be executed due to current device
-222, "Data out of range"	A legal program data element was parsed but could not be executed because the value was outside the legal range as defined by the device.
-224, "Illegal parameter value"	Used where exact value, from a list of possible values, was expected.

Error/Event Code	Description
-400, "Query error"	Generic query error as defined in IEEE 488.2
-500, "Power on"	The instrument has detected an off to on transition in its power supply.
-600, "User request"	This event occurs when the instrument detects the activation of a user request local control.
-800, "Operation complete"	The instrument has completed all selected pending operations in accordance with the IEEE 488, 12.5.2 synchronization protocol.
-350, "Queue overflow"	If the queue overflows the last event/error in the queue is replaced with this error.

6.10.1 "Settings Conflict" Used for Settings Dependencies

As described in 3.21 Working with Setting Dependencies, the N4960A serial BERT controller has a number of settings which have a dependency on another setting.

From the front panel, the user is warned of these restrictions, and is given the opportunity to clear the conflict and carry out the user's request. However, the programming interface is not conducive to that behavior. Instead, the programming interface generates the "Settings Conflict" SCPI error if the controlling program has requested a value that cannot be achieved due to other dependent settings. For example, if the controlling program enables both SJ1 and SJ2, sets SJ1 to 0.4 UI, and then attempts to set SJ2 to 0.7 UI, the "Settings Conflict" error message will be generated.

The one exception to this rule is the relationship between PJ Frequency and PJ Amplitude. The PJ Amplitude is a function of the PJ Frequency. If the controlling program attempts to change the PJ Frequency such that it is incompatible with the current PJ Amplitude, the N4960A serial BERT controller will respond with a AMPL_LIMIT_WARN instrument non-fatal error message (see Table 22), but will grant the PJ Frequency requested and set the PJ Amplitude to within valid range.

6.11 N4960A Serial BERT Controller Device Commands

Command

:OUTDelay:AMPLitude

Description

Set the amplitude of the output delay logic level from 0.3 V to 1.7 V in 0.005 V increments. The optional units are V (default) and mV. The default value is 0.7 V.

Example

:OUTD:AMPL 750mV

Command

:OUTDelay:AMPLitude?

Description

Return the amplitude value of the output delay logic level. The range is 0.3 V to 1.7 V.

Example

:OUTD:AMPL?
0.750V

Command

:OUTDelay:COUPling

Description

Set the position of the internal switch to AC (default) or DC. Offset or termination must be set to 0 V to change coupling to AC or a setting conflict error message will be generated. If coupling is already set to AC, it can be changed to DC without any dependencies.

Example

:OUTD:COUP DC

Command

:OUTDelay:COUPling?

Description

Return the position of the internal switch. The returned string is AC or DC.

Example

:OUTD:COUP?
DC

Command

:OUTDelay:DELay

Description

Set the precision delay value of the clock output from -1000 UI to 1000 UI in 0.001 UI increments. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0 UI.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number "1"). The *OPC? query command can be appended to the command as shown below.

Example

```
:OUTD:DEL 1;*OPC?
1
```

Command

:OUTDelay:DELay?

Description

Return the value of the output delay. The data delay range is –1000 UI to 1000 UI.

Example

```
:OUTD:DEL?
1.000UI
```

Command

:OUTDelay:OFFSet

Description

Set the offset voltage of the output delay logic level from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

If the desired offset voltage is incompatible with the current termination voltage, a setting conflict error message will be generated and the offset cannot be set.

If the offset is changed to a value other than 0 V while the coupling is set to AC, a setting conflict error message will be generated and the offset cannot be set. If the coupling is set to DC, then offset can be changed.

Example

:OUTD:OFFS 2V

Command

:OUTDelay:OFFSet?

Description

Return the offset value of the output delay logic level. The range is –2.4 V to +2.4 V.

Example

:OUTD:OFFS?
2.000V

Command

:OUTDelay:OUTPut

Description

Turn the output delay clock ON or OFF. The default is OFF.

Example

:OUTD:OUTP on

Command

:OUTDelay:OUTPut?

Description

Return the status of the output delay clock. The returned string is either ON or OFF.

Example

:OUTD:OUTP?
ON

Command

:OUTDelay:TERMination

Description

Set the termination voltage of the output delay logic level from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

If the desired termination voltage is incompatible with the current offset voltage, a setting conflict error message will be generated and the termination cannot be set.

If the termination is changed to a value other than 0 V while the coupling is set to AC, a setting conflict error message will be generated and the termination cannot be set. If the coupling is set to DC, then termination can be changed.

Example

:OUTD:TERM 1.3V

Command

:OUTDelay:TERMination?

Description

Return the termination value of the output delay logic level. The range is –2.4 V to +2.4 V.

Example

:OUTD:TERM?
1.300V

Command

:OUTJitter:AMPLitude

Description

Set the amplitude of the clock signal at the clock outputs from 0.3 V to 1.7 V in 0.005 V increments. The optional units are V (default) and mV. The default value is 0.7 V.

Example

:OUTJ:AMPL 750mV

Command

:OUTJitter:AMPLitude?

Description

Return the amplitude of the clock signal at the clock outputs. The range is 0.3 V to 1.7 V.

Example

:OUTJ:AMPL?
0.750V

Command

:OUTJitter:COUPling

Description

Set the position of the internal switch to AC (default) or DC. Offset or termination must be set to 0 V to change coupling to AC or a setting conflict error message will be generated. If coupling is already set to AC, it can be changed to DC without any dependencies.

Example

:OUTJ:COUP DC

Command

:OUTJitter:COUPling?

Description

Return the status of the internal switch. The returned string is AC or DC.

Example

:OUTJ:COUP?
DC

Command

:OUTJitter:JITTer:EXTernal

Description

Set jitter measurements to be made using a high or high deviation path. The settings are OFF, HIGHband or LOWband. The default is OFF.

Sinusoidal 1 jitter, Sinusoidal 2 jitter, random jitter, and external jitter (low deviation) can be enabled simultaneously. The Sinusoidal periodic jitter path or external high deviation jitter path cannot be enabled if any of the other jitter paths are enabled or a setting conflict error message will be generated.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

:OUTJ:JITT:EXT high;*OPC?
1

Command

:OUTJitter:JITTer:EXTernal?

Description

Return the status of the external jitter source band. The returned string is OFF, HIGHband, or LOWband.

Example

:OUTJ:JITT:EXT?
HIGH

Command

:OUTJitter:JITTer:EXTernal:LBGain

Description

Set the external low band range from 0.001 UI/V to 50 UI/V in 0.001 UI/V increments. The optional units are UI/V (Unit Interval) and mUI/V (milli Unit Interval). The default value/unit is 1 UI/V.

Example

:OUTJ:JITT:EXT:LBG 2UI/V;*OPC?
1

Command

:OUTJitter:JITTer:EXTernal:LBGain?

Description

Return the value of the external low band amplitude. The range is 0.001 UI/V to 50 UI/V.

Example

.:OUTJ:JITT:EXT:LBG?
2.000UI/V

Command

:OUTJitter:JITTer:PERiodic

Description

Turn the periodic jitter output ON or OFF. The default is OFF.

Periodic jitter cannot be enabled if any of the other jitter sources are enabled.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

```
:OUTJ:JITT:PER ON;*OPC?
1
```

Command

:OUTJitter:JITTer:PERiodic?

Description

Return the status of the periodic jitter. The returned string is either ON or OFF.

Example

```
:OUTJ:JITT:PER?
ON
```

Command

:OUTJitter:JITTer:PERiodic:AMPLitude

Description

Set the periodic jitter level from 0 UI to 100 UI in 0.001 UI increments. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0.001 UI. The PJ amplitude range is a function of PJ frequency.

NOTE SCPI values related to UI, such as jitter amplitude or delay, must be set to half of the value desired on the pattern generator outputs or error detector delay.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

```
:OUTJ:JITT:PER:AMP 1UI;*OPC?
1
```

Command

:OUTJitter:JITTer:PERiodic:AMPLitude?

Description

Return the value of the periodic jitter amplitude. The range is 0 UI to 100 UI.

Example

```
:OUTJ:JITT:PER:AMP?
1.000UI
```

Command

:OUTJitter:JITTer:PERiodic:FREQuency

Description

Set the periodic jitter frequency from 1 Hz to 17 MHz in 1 Hz increments. The optional units are Hz, kHz, MHz, and GHz. The default value/unit is 100000 Hz. The PJ amplitude range is a function of PJ frequency. If the frequency is changed to a value incompatible with the current amplitude, the amplitude will automatically be adjusted to fit the range deviated by the desired frequency and a data out of range error will be generated.

Example

:OUTJ:JITT:PER:FREQ 4MHz

Command

:OUTJitter:JITTer:PERiodic:FREQuency?

Description

Return the value of the periodic jitter frequency. The range is 1 Hz to 17 MHz.

Example

:OUTJ:JITT:PER:FREQ?
4000000 Hz

Command

:OUTJitter:JITTer:RANDom

Description

Enable (ON) or disable (OFF) random jitter on the jittered clock outputs. The default is OFF.

SJ1, SJ2, RJ, and external jitter (low deviation) can be enabled simultaneously. RJ cannot be enabled if PJ or external jitter (lowband) is enabled or a setting conflict error message is generated.

Example

:OUTJ:JITT:RAND on

Command

:OUTJitter:JITTer:RANDom?.

Description

Return the status of the random jitter source. The returned string is either ON or OFF.

Example

:OUTJ:JITT:RAND?
ON

Command

:OUTJitter:JITTer:RANDom:AMPLitude

Description

Set the random jitter level from 0 UI-rms to 0.150 UI-rms in 0.001 UI-rms increments. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range. The optional units are UI-rms (Unit Interval-rms) and mUI-rms (milli Unit Interval). The default value/unit is 0 UI-rms.

NOTE **SCPI values related to UI, such as jitter amplitude or delay, must be set to half of the value desired on the pattern generator outputs or error detector delay.**

Example

:OUTJ:JITT:RAND:AMPL .1UI-RMS

Command

:OUTJitter:JITTer:RANDom:AMPLitude?

Description

Return the value of the random level. The range is 0 UI-rms to 0.150 UI-rms. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range.

Example

:OUTJ:JITT:RAND:AMPL?
0.100UI-rms

Command

:OUTJitter:JITTer:SINusoidal1

Description

Turn the SJ1 output ON or OFF. The default is OFF.

SJ1, SJ2, RJ, and external jitter (low deviation) can be enabled simultaneously. SJ1 and SJ2 cannot be enabled if PJ or external jitter (lowband) is enabled or a setting conflict error message will be generated.

Example

:OUTJ:JITT:SIN1 on

Command

:OUTJitter:JITTer:SINusoidal1?

Description

Return the status of SJ1. The returned string is either ON or OFF.

Example

:OUTJ:JITT:SIN1?
ON

Command

:OUTJitter:JITTer:SINusoidal1:AMPLitude

Description

Set the SJ1 level from 0 UI to 1.0 UI in 0.001 UI increments. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0 UI.

If SJ2 is enabled, the sum of SJ1 and SJ2 cannot exceed 1.0 UI or a setting conflict error message is generated.

NOTE **SCPI values related to UI, such as jitter amplitude or delay, must be set to half of the value desired on the pattern generator outputs or error detector delay.**

Example

:OUTJ:JITT:SIN1:AMPL 1UI

Command

:OUTJitter:JITTer:SINusoidal1:AMPLitude?

Description

Return the value of the SJ1 amplitude. The range is 0 UI to 1.0 UI. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range.

Example

:OUTJ:JITT:SIN1:AMPL?
1.000UI

Command

:OUTJitter:JITTer:SINusoidal1:FREQuency

Description

Set the SJ1 frequency from 1 Hz to 200 MHz in 1 Hz increments. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range. The optional units are Hz, kHz, MHz, and GHz. The default value/unit is 10000000 Hz.

Example

:OUTJ:JITT:SIN1:FREQ 100MHz

Command

:OUTJitter:JITTer:SINusoidal1:FREQuency?

Description

Return the value of the SJ1 frequency. The range is 1 Hz to 200 MHz. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range.

Example

:OUTJ:JITT:SIN1:FREQ?
100000000 Hz

Command

:OUTJitter:JITTer:SINusoidal2

Description

Turn the sinusoidal 2 jitter output ON or OFF. The default is OFF.

SJ1, SJ2, RJ, and external jitter (low deviation) can be enabled simultaneously.

SJ1 and SJ2 cannot be enabled if PJ or external jitter (lowband) is enabled or a setting conflict error message will be generated.

Example

:OUTJ:JITT:SIN2 on

Command

:OUTJitter:JITTer:SINusoidal2?

Description

Return the status of SJ2. The returned string is either ON or OFF.

Example

:OUTJ:JITT:SIN2?
ON

Command

:OUTJitter:JITTer:SINusoidal2:AMPLitude

Description

Set the SJ2 level from 0 UI to 1.0 UI in 0.001 UI increments. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0 UI.

If SJ1 is enabled, the sum of SJ1 and SJ2 cannot exceed 1.0 UI or a setting conflict error message is generated.

NOTE **SCPI values related to UI, such as jitter amplitude or delay, must be set to half of the value desired on the pattern generator outputs or error detector delay.**

Example

:OUTJ:JITT:SIN2:AMPL 1UI

Command

:OUTJitter:JITTer:SINusoidal2:AMPLitude?

Description

Return the value of the SJ2 amplitude. The range is 0 UI to 1.0 UI. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range.

Example

:OUTJ:JITT:SIN2:AMPL?
1.000UI

Command

:OUTJitter:JITTer:SINusoidal2:FREQuency

Description

Set the SJ2 frequency from 1 Hz to 200 MHz in 1 Hz increments. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range. The optional units are Hz, kHz, MHz, and GHz. The default value/unit is 10000000 Hz.

Example

:OUTJ:JITT:SIN2:FREQ 100MHz

Command

:OUTJitter:JITTer:SINusoidal2:FREQuency?

Description

Return the value of the SJ2 frequency. The range is 1 Hz to 200 MHz. This is the over-programming range. Refer to 5 Performance Specifications for the maximum specified range.

Example

:OUTJ:JITT:SIN2:FREQ?
100000000 Hz

Command

:OUTJitter:OFFSet

Description

Set the DC offset voltage at the clock outputs from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value is 0 V.

If the desired offset voltage is incompatible with the current termination voltage, a setting conflict error message will be generated and the offset cannot be set.

If the offset is changed to a value other than 0 V while the coupling is set to AC, a setting conflict error message will be generated and the offset cannot be set. If the coupling is set to DC, then offset can be changed.

Example

:OUTJ:OFFS 2V

Command

:OUTJitter:OFFSet?

Description

Return the DC offset voltage at the clock outputs. The range is –2.4 V to +2.4 V.

Example

:OUTJ:OFFS?
2.000V

Command

:OUTJitter:OUTPut

Description

Turn the output jitter clock ON or OFF. The default is OFF.

Example

:OUTJ:OUTP on

Command

:OUTJitter:OUTPut?

Description

Return the status of the output jitter clock. The returned string is either ON or OFF.

Example

:OUTJ:OUTP?
ON

Command

:OUTJitter:TERMination

Description

Set the DC output offset of the clock output to support the specified termination voltage of the 50Ω input port from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

If the desired termination voltage is incompatible with the current offset voltage, a setting conflict error message will be generated and the termination cannot be set.

If the termination is changed to a value other than 0 V while the coupling is set to AC, a setting conflict error message will be generated and the termination cannot be set. If the coupling is set to DC, then termination can be changed.

Example

:OUTJ:TERM 1.3V

Command

:OUTJitter:TERMination?

Description

Return the termination voltage of the 50 Ω input port. The range is –2.4 V to +2.4 V.

Example

:OUTJ:TERM?
1.300V

Command

:OUTSubrate:AMPLitude

Description

Set the amplitude of the divided clock output logic level from 0.3 V to 1.7 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0.7 V.

Example

:OUTS:AMPL 750mV

Command

:OUTSubrate:AMPLitude?

Description

Return the amplitude value of the divided clock output logic level. The range is 0.3 V to 1.7 V.

Example

:OUTS:AMPL?
0.750V

Command

:OUTSubrate:COUPling

Description

Set the position of the internal switch to AC (default) or DC. Offset or termination must be set to 0 V to change coupling to AC or a setting conflict error message will be generated. If coupling is already set to AC, it can be changed to DC without any dependencies.

Example

:OUTJ:COUP DC

Command

:OUTSubrate:COUPling?

Description

Return the status of the internal switch. The returned string is AC or DC.

Example

:OUTJ:COUP?
DC

Command

:OUTSubrate:DIVider

Description

Set the divider value for the divided clock output from 1 to 99999999 in increments of 1. The default value is 4.

Example

:OUTS:DIV 6

Command

:OUTSubrate:DIVider?

Description

Return the divider value. The range is 1 to 99999999.

Example

:OUTS:DIV?
6

Command

:OUTSubrate:OFFSet

Description

Set the offset voltage of the divided clock output logic level from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

If the desired offset voltage is incompatible with the current termination voltage, a setting conflict error message will be generated and the offset cannot be set.

If the offset is changed to a value other than 0 V while the coupling is set to AC, a setting conflict error message will be generated and the offset cannot be set. If the coupling is set to DC, then offset can be changed.

Example

:OUTS:OFFS 2V

Command

:OUTSubrate:OFFSet?

Description

Return the offset value of the divided clock output logic level. The range is –2.4 V to +2.4 V.

Example

:OUTS:OFFS?
2.000V

Command

:OUTSubrate:OUTPut

Description

Turn the divided clock output ON or OFF. The default is OFF.

Example

:OUTS:OUTP on

Command

:OUTSubrate:OUTPut?

Description

Return the status of the divided clock output. The returned string is either ON or OFF.

Example

:OUTS:OUTP?
ON

Command

:OUTSubrate:TERMination

Description

Set the termination voltage of the divided clock output logic level from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

If the desired termination voltage is incompatible with the current offset voltage, a setting conflict error message will be generated and the termination cannot be set.

If the termination is changed to a value other than 0 V while the coupling is set to AC, a setting conflict error message will be generated and the termination cannot be set. If the coupling is set to DC, then termination can be changed.

Example

:OUTS:TERM 1.3V

Command

:OUTSubrate:TERMination?

Description

Return the termination value of the subrate output logic level. The range is –2.4 V to +2.4 V.

Example

:OUTS:TERM?
1.300V

Command

:SOURce:DCLock:FREQuency

Description

Set the external delay clock frequency from 1 to 16 GHz (without remote heads connected) in 1 kHz increments. The optional units are Hz, kHz, MHz, and GHz. The default value/unit is 5 GHz. Refer to 5 Performance Specifications for clock frequency range with remote heads connected.

Frequency can only be set when :SOURce:DCLock:PATH is set to EXTernal.

Example

:SOUR:DCL:FREQ 2.5GHz

Command

:SOURce:DCLock:FREQuency?

Description

Return the value of the external delay clock frequency.

If :SOURce:DCLock:PATH is set to SYSTem, then the frequency of the internal clock is returned. The default is the frequency value of the internal clock.

Example

:SOUR:DCL:FREQ?
2500MHz

Command

:SOURce:DCLock:PATH

Description

Set the delay clock path to SYSTem for using the internal delay clock source or EXTernal for using an external delay clock source. The default is SYSTem.

Example

:SOUR:DCL:PATH SYST

Command

:SOURce:DCLock:PATH?

Description

Return the status of the delay clock source path. The returned string is either SYST (internal delay source) or EXT (external delay source).

Example

:SOUR:DCL:PATH?
SYST

Command

:SOURce:FREQuency

Description

Set the internal clock frequency from 1 to 16 GHz (without remote heads connected) in 1 kHz increments. The optional units are Hz, kHz, MHz, and GHz. The default value/unit is 5 GHz. Refer to 5 Performance Specifications for clock frequency range with remote heads connected.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

NOTE The N4951A or N4951B pattern generators require up to 4 seconds for the output to settle following a frequency change.

Example

```
:SOUR:FREQ 2.5GHz;*OPC?
1
```

Command

:SOURce:FREQuency?

Description

Return the value of the internal clock frequency. The range is 1 to 16 GHz (without remote heads connected).

Example

```
:SOUR:FREQ?
2500000000 Hz
```

Command

:SOURce:FREQuency:CW

Description

Set the internal clock CW frequency from 1 to 16 GHz (without remote heads connected) in 1 kHz increments. The optional units are Hz, kHz, MHz, and GHz. The default unit is Hz. Refer to 5 Performance Specifications for clock frequency range with remote heads connected.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

```
:SOUR:FREQ:CW 2.5GHz;*OPC?
1
```

Command

:SOURce:FREQuency:CW?

Description

Return the value of the source CW frequency. The range is 1 to 16 GHz.

Example

```
:SOUR:FREQ:CW?
2500000000 Hz
```

Command

:SOURce:FREQuency:PATH

Description

Set the frequency path to INTernal for using the internal source or EXTernal for using an external source. The default is INTernal. The N4960A BERT Controller should be disabled before setting the clock source to EXTernal.

If spread spectrum clock (SSC) is enabled, then a setting conflict error message will be generated and the clock source cannot be set to EXTernal.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

```
:SOUR:FREQ:PATH INT;*OPC?
1
```

NOTE If the clock source is set to External without a valid clock signal connected, then the results from the :SOUR:FREQ? query may fluctuate or return “0000 Hz”. In addition, a “FREQ/OOR” (frequency out of range) error may be generated. If either of these conditions is detected, check the external clock source.

Command

:SOURce:FREQuency:PATH?

Description

Return the status of the source frequency path. The returned string is either INT (internal source) or EXT (external source).

Example

:SOUR:FREQ:PATH?
INT

Command

:SOURce:ROSCillator:PATH

Description

Set the frequency path of the reference oscillator to AUTO for sensing the reference source automatically, INTernal for using the internal reference source, or EXTernal for using an external reference source. The default is AUTO.

Example

:SOUR:ROSC:PATH EXT

NOTE If the 10 MHz Reference is set to Auto mode, whenever it switches between Internal and External, a message indicating the switch is generated ("REF,INTERNAL" and "REF,EXTERNAL") respectively. If the 10 MHz Reference is using an External source and there is a loss of signal, a loss of signal error will be generated ("REF,LOS").

Command

:SOURce: ROSCillator:PATH?

Description

Return the status of the reference oscillator source frequency path. The returned string is AUTO (detect source automatically), INT (internal source), or EXT (external source).

Example

:SOUR:ROSC:PATH?
EXT

Command

:SOURce:SSCLocking

Description

Turn the spread spectrum clock (SSC) ON or OFF. The default is OFF. The clock source must be set to INTernal before enabling the N4960A Serial BERT 17 and 32 Gb/s. If the clock source is set to EXTernal, a setting conflict error message is generated and SSC cannot be enabled.

Example

:SOUR:SSCL on

Command

:SOURce:SSCLocking?

Description

Return the status of the spread spectrum clock. The returned string is either ON or OFF.

Example

:SOUR:SSCL?
ON

Command

:SOURce:SSCLocking:DEViation

Description

Set the spread spectrum clock deviation from 0 PPM (parts per million) to 10000 PPM in 1 PPM increments. The default value/unit is 5000 PPM.

Example

:SOUR:SSCL:DEV 10000ppm

Command

:SOURce:SSCLocking:DEViation?

Description

Return the deviation value of the spread spectrum clock. The range is 0 PPM (parts per million) to 10000 PPM.

Example

:SOUR:SSCL:DEV?
10000PPM.

Command

:SOURce:SSCLocking:FREQuency

Description

Set the spread spectrum clock frequency from 1 Hz to 50000 Hz in 1 Hz increments. The optional units are Hz and kHz. The default value/unit is 33000 Hz.

Example

:SOUR:SSCL:FREQ 50kHz

Command

:SOURce:SSCLocking:FREQuency?

Description

Return the value of the spread spectrum clock frequency. The range is 1 Hz to 50000 Hz.

Example

:SOUR:SSCL:FREQ?
50000 Hz

Command

:SOURce:SSCLocking:TYPE

Description

Set the spread spectrum clock direction to DOWN, UP, or CENTer. The default is DOWN.

Example

:SOUR:SSCL:TYPE UP

Command

:SOURce:SSCLocking:TYPE?

Description

Return the status of the spread spectrum clock type. The returned string is DOWN, UP, or CENTer.

Example

:SOUR:SSCL:TYPE?
UP

Command

:SYSTem:DATE

Description

Set the current date. The format is YYYY,MM,DD.

Command

:SYSTem:DATE?

Description

Return the current date.

Example

:SYST:DATE?
2011,09,02

Command

:SYSTem:ERRor?

Description

Responds with oldest Event/Error Log Report from the queue and removes it from the list of unread messages.

Example

:SYST:ERR?
-222, “Data out of range”

Command

:SYSTem:ERRor:ALL?

Description

Return all Event/Error Log Reports (read and unread).

Example

:SYST:ERR:ALL?
-100, “Command error”, -222, “Data out of range”,
-224, “Illegal parameter value”

Command

:SYSTem:ERRor:COUNt?

Description

Query the error/event queue for the number of unread items. As errors and events may occur at any time, more items may be present in the queue at the time it is read. If the queue is empty, the response is 0.

Example

:SYST:ERR:COUN?

Command

:SYSTem:ERRor:NEXT?

Description

Return the next Event/Error code. If the event/error queue of unread error messages is empty, the response is 0.

Example

:SYST:ERR:NEXT?
0, ”No error”

Command

:SYSTem:HEADs?

Description

Queries the system for the currently connected remote heads and returns the type, hardware version, firmware version, and serial number. The serial number format is country (2 characters), year (number of years after 1960), week number (2 digits), and sequence number (4 digits).

Example

:SYST:HEAD?
N4951A-P32,02.00,03.00.00.20,US52340206:N4952A-E32,02.00,03.00.01.02, US52340224:

Command

:SYSTem:LLOCkout

Description

Place the instrument in local lockout (remote mode) with front panel locked out. The user must use the below command to set the instrument back to local or power down to re-start the instrument.

Example

:SYST:LLOC
The following message is displayed on the front panel:
LOCAL LOCKOUT
FRONT PANEL DISABLED.

Command

:SYSTem:LOCal

Description

Places instrument from local lockout to local mode.

Example

:SYST:LOC

Command

:SYSTem:PRESet

Description

Execute a system preset. This command is the same as pressing the front panel Preset key.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

```
:SYSTem:PRESet;*OPC?
1
```

Command

:SYSTem:STATe:RECall

Description

Recall a previously saved state from 1 to 5.

Command

:SYSTem:STATe:SAVE

Description

Save a system state to a storage number from 1 to 5.

Command

:SYSTem:TIME

Description

Set the current time. The format is HH,MM,SS.

Command

:SYSTem:TIME?

Description

Return the current time.

Command

:SYSTem:VERSion?

Description

Return current version of SCPI commands.

Example

:SYST:VERS?
1999.0

6.12 Pattern Generator Device Commands

NOTE Jitter and spread spectrum clock can only be set using the N4960A serial BERT controller clock SCPI commands. Therefore, SCPI values must be set to half of the value desired on the pattern generator outputs.

NOTE Commands for controlling a pattern generator are preceded by :PG. However, legacy commands preceded by :PG17 or :PG32 are supported but not recommended.

NOTE Commands can be sent to a pattern generator currently connected to channel 0 (Jitter), channel 1 (Delay), or both. Refer to **6.8 Pattern Generator Channelization** for information about how to send commands to the intended pattern generator.

Command

:PG:DATA:DEEMphasis:POST1

Description

Set the 5-tap data de-emphasis POST1 cursor from 0 to –30 dB in 0.1 dB increments. The optional unit is dB. This command applies to the N4951B-D17/-D32 only.

Example

:PG:DATA:DEEM:POST1 –3 (@ 0)
Sets the postcursor 1 to –3 dB for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:DEEMphasis:POST1?

Description

Return the value of the 5-tap data de-emphasis POST1 cursor. The de-emphasis range is –30 dB to 0 dB. This command applies to the N4951B-D17/-D32 only.

Example

:PG:DATA:DEEM:POST1? (@ 0)
–3.0dB
Queries the postcursor 1 setting for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:DEEMphasis:POST2

Description

Set the 5-tap data de-emphasis POST2 cursor from –30 dB to +30 dB (relative to post-cursor1) in 0.1 dB increments. The optional unit is dB. This command applies to the N4951B-D17/-D32 only.

Example

:PG:DATA:DEEM:POST2 0
Sets the postcursor 2 to 0 dB for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:DEEMphasis:POST2?

Description

Return the value of the 5-tap data de-emphasis POST2 cursor. The de-emphasis range is –30 dB to +30 dB. This command applies to the N4951B-D17/-D32 only.

Example

:PG:DATA:DEEM:POST2?
0dB
Queries the postcursor 2 setting for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:DEEMphasis:POST3

Description

Set the 5-tap data de-emphasis POST3 cursor from –30 dB to +30 dB (relative to post-cursor1) in 0.1 dB increments. The optional unit is dB. This command applies to the N4951B-D17/-D32 only.

Example

:PG:DATA:DEEM:POST3 0
Sets the postcursor 3 to 0 dB for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:DEEMphasis:POST3?

Description

Return the value of the 5-tap data de-emphasis POST3 cursor. The de-emphasis range is –30 dB to +30 dB. This command applies to the N4951B-D17/-D32 only.

Example

:PG:DATA:DEEM:POST3?
0dB
Queries the postcursor 3 setting for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:DEEMphasis:PRECursor

Description

Set the 5-tap data de-emphasis PRECursor from 0 dB to +30 dB in 0.1 dB increments. The optional unit is dB. This command applies to the N4951B-D17/-D32 only.

Example

:PG:DATA:DEEM:PREC 0 (@ 0)
Sets the precursor to 0 dB for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:DEEM:PRECursor?

Description

Return the value of the 5-tap data de-emphasis PRECursor. The de-emphasis range is 0 dB to +30 dB. This command applies to the N4951B-D17/-D32 only.

Example

:PG:DATA:DEEM:PREC? (@ 0)
0.0dB
Queries the precursor setting for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:LLEVel

Description

Set the data logic level. Selecting a logic level defines a commonly understood output amplitude, offset, and termination voltage. Editing any parameter will automatically change the logic level to “CUSTom”. The default is CUSTom. The options are shown in Table 34.

Table 34. Data logic levels

Logic Family	Amplitude	Offset	Termination
LVPECL	0.8 V	2.0 V	1.3 V
LVDS	0.4 V	1.25 V	1.25 V
ECL	0.8 V	-1.3 V	-2.0 V

Example

:PG:DATA:LLEV lvpecl (@ 0:1)
Sets the logic level to LVPECL on pattern generators connected to channel 0 (Jitter) and channel 1 (Delay).

Command

:PG:DATA:LLEVel?

Description

Return the status of the logic level. The returned string will be LVPECL, LVDS, ECL, or CUST.

Example

:PG:DATA:LLEV? (@ 0:1)
LVPECL, LVPECL
Queries the logic level of the pattern generators connected to channel 0 (Jitter) and channel 1 (Delay).

Command

:PG:DATA:LLEVel:AMPLitude

Description

Adjust the amplitude of the data eye presented at the data outputs from 0.1 V to 1 V (N4951A), 0.3 V to 3.0 V (N4951B-H17/H32), or 0.3 V to 1.5 V (N4951B-D17/D32) in 0.005 V increments. This is the single ended amplitude. The units are V and mV. The default value/unit is 0.5 V.

Example

:PG:DATA:LLEV:AMPL 800mV
Sets the amplitude to 800 mV for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:LLEVel:AMPLitude?

Description

Return the amplitude value of the data logic level.

Example

:PG:DATA:LLEV:AMPL?
0.800V
Queries the amplitude of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:LLEVel:OFFSet

Description

Adjust the DC offset of the data eye presented at the data outputs from –2.0 V to 2.0 V in 0.005 V increments. The units are V and mV. The default value/unit is 0.0 V.

Example

:PG:DATA:LLEV:OFFS 2V (@ 1)
Sets the DC offset to 2 V for the pattern generator connected to channel 1 (Delay) only.

Command

:PG:DATA:LLEVel:OFFSet?

Description

Return the DC offset value of the data logic level.

Example

:PG:DATA:LLEV:OFFS? (@ 1)
2.000V
Queries the DC offset of the pattern generator connected to channel 1 (Delay) only.

Command

:PG:DATA:LLEVel:TERMination

Description

Set the DC output offset of the data eye to support a specified termination voltage of a DUT having a 50 Ω input port. The range is –2.0 V to 2.0 V in 0.005 V increments. The units are V and mV. The default value/unit is 0.0 V.

Example

:PG:DATA:LLEV:TERM 1.3V (@ 0)
Sets the termination voltage to 1.3 V for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:LLEVel:TERMination?

Description

Return the termination value of the data logic level.

Example

:PG:DATA:LLEV:TERM? (@ 0)
1.300V
Queries the termination voltage of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:OUTPut

Description

Turn the pattern generator data outputs ON or OFF. The default is OFF upon cycling the power, executing a *RST command, or performing an instrument preset.

Example

:PG:DATA:OUTP on (@ 0,1)
Sets the data outputs to on for the pattern generators connected to channel 0 (Jitter) and channel 1 (Delay).

Command

:PG:DATA:OUTPut?

Description

Return the status of the pattern generator data outputs. The returned string is either ON or OFF.

Example

:PG:DATA:OUTP? (@ 0,1)
ON, ON
Queries the status of the data outputs of the pattern generators connected to channel 0 (Jitter) and channel 1 (Delay).

Command

:PG:DATA:OUTPut:DELay

Description

Set the pattern generator delay in channel 1 from –2000 UI to 2000 UI in 0.002 UI increments. This sets the amount the clock is shifted to align the pattern in the channel 1 (Delay) path. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0.00 UI.

NOTE Delay value specified using this command will be the value on the pattern generator outputs.

NOTE This command affects channel 1 (Delay) only. Channel 1 must be specified or the command will be sent to channel 0 (Jitter) and an error will be returned.

Example

:PG:DATA:OUTP:DEL 1000UI (@ 1)
Sets the delay to 1000UI for the pattern generator connected to channel 1 (Delay) only.

Command

:PG:DATA:OUTPut:DELay?

Description

Return the delay value. The range is –2000 UI to 2000 UI.

Example

:PG:DATA:OUTP:DEL? (@ 1)
1000UI
Queries the delay value of the pattern generator connected to channel 1 (Delay).

Command

:PG:DATA:PATTern:ERRInjection

Description

Set the continuous error injection ON or OFF. Single errors can be injected even when this command is set to OFF. The rate is set using the :PG:DATA:PATTern:ERRInjection:RATE command.

Example

:PG:DATA:PATT:ERRI on
Sets the error injection to on for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:ERRInjection?

Description

Return the state of the error injection. The returned string will be ON or OFF.

Example

:PG:DATA:PATT:ERRI?
ON
Queries the error injection state of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:ERRInjection:RATE

Description

Set the error injection rate. The error injection rates are as follows:
E-3
E-4
E-5
E-6
E-7
E-8
E-9

The default is E-3 (at least 1 error bit in 1000 bits).

Example

:PG:DATA:PATT:ERRI:RATE E-6
Sets the error injection to 1 error bit in 1000000 bits for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:ERRInjection:RATE?

Description

Return the error injection rate value. The error injection rates are as follows:
E-3
E-4
E-5
E-6
E-7
E-8
E-9

Example

:PG:DATA:PATT:ERRI:RATE?
E-6
Queries the error injection rate value of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:ERRInjection:SINGle

Description

Inject a single error. A single error can be injected regardless of whether error injection is on or off.

Example

:PG:DATA:PATT:ERRI:SING (@ 1)
Injects a single error from the pattern generator connected to channel 1 (Delay).

Command

:PG:DATA:PATTern:LIST:FACTory?

Description

Return the list of all available factory patterns. These patterns have a filename containing eight characters with a three character extension (.fpt).

Example

:PG:DATA:PATT:LIST:FACT?
10.FPT, 1100.FPT, 111000.FPT, 11110000.FPT, 81s_80s.FPT, 161_160.FPT, 321_320.FPT, 641_640.FPT, CJPAT.FPT, CJTPAT.FPT, CRPAT.FPT, JSPAT.FPT, JTSPAT.FPT, K28-3.FPT, K28-5.FPT, K28
Queries the list of factory patterns of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:LIST:PRBS?

Description

Return the list of all available PRBS hardware patterns.

Example

:PG:DATA:PATT:LIST:PRBS?
PRBS2^7-1, PRBS2^9-1, PRBS2^10-1, PRBS2^11-1, PRBS2^15-1, PRBS2^23-1, PRBS2^29-1, PRBS2^31-1, PRBS2^33-1, PRBS2^35-1, PRBS2^39-1, PRBS2^41-1, PRBS2^45-1, PRBS2^47-1, PRBS2^49-1, PRBS2^51-1
Queries the list of PRBS patterns of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:LIST:USER?

Description

Return the list of all available user patterns, which are the patterns created via the N4980A multi-instrument BERT software and uploaded to the N4960A serial BERT controller. These patterns have a filename containing eight characters with a three character extension (.usr).

Example

:PG:DATA:PATT:LIST:USER?
Queries the list of user patterns of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:NAME

Description

Select the data pattern name. The default is PRBS2^7-1. The list of PRBS and factory patterns are as follows:

PRBS2^7-1, PRBS2^9-1, PRBS2^10-1, PRBS2^11-1, PRBS2^15-1, PRBS2^23-1, PRBS2^29-1, PRBS2^31-1, PRBS2^33-1, PRBS2^35-1, PRBS2^39-1, PRBS2^41-1, PRBS2^45-1, PRBS2^47-1, PRBS2^49-1, PRBS2^51-1, 10.FPT, 1100.FPT, 111000.FPT, 11110000.FPT, 81s_80s.FPT, 161_160.FPT, 321_320.FPT, 641_640.FPT, CJPAT.FPT, CJTPAT.FPT, CRPAT.FPT, JSPAT.FPT, JTSPAT.FPT, K28-3.FPT, K28-5.FPT,K28-7.FPT.

NOTE

This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

:PG:DATA:PATT:NAME PRBS2^7-1;*OPC?
1
Selects the pattern name for the pattern generator connected to channel 0 (Jitter) only and uses the *OPC? query command to determine if the operation is complete.

Command

:PG:DATA:PATTern:NAME?

Description

Return the selected data pattern name.

Example

:PG:DATA:PATT:NAME?
 PRBS2^7-1
Queries the selected pattern name of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:POLarity

Description

Set the data pattern polarity to INVert, to invert the data pattern presented at the data outputs, or NONInvert. The default is NONInvert.

Example

:PG:DATA:PATT:POL INV
Sets the pattern polarity to inverted for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:PATTern:POLarity?

Description

Return the data pattern polarity. The returned string is either INV or NONI.

Example

:PG:DATA:PATT:POL?
INV
Queries the pattern polarity of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:XOVer

Description

Set the data crossover from 35% to 65% in 1% increments (integers only). The default is 50%.

Example

:PG:DATA:XOV 35
Sets the crossover to 35% for the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DATA:XOVer?

Description

Return the data crossover value. The data crossover range is 35% to 65%.

Example

:PG:DATA:XOV?
35%
Queries the crossover value of the pattern generator connected to channel 0 (Jitter) only.

Command

:PG:DRATe?

Description

Return the current data rate. The data rate is two times the clock frequency.

Example

:PG:DRATe?
10000000000 bps
Queries the current data rate of the pattern generator connected to channel 0 (Jitter) only.

6.13 Error Detector Device Commands

NOTE Commands for controlling an error detector are preceded by :ED. However, legacy commands preceded by :ED17 or :ED32 are supported but not recommended. Commands preceded with :ED can be sent to a 17 Gb/s error detector or 32 Gb/s error detector.

Command

:ED:DATA:AALign:CAALign:DELay

Description

Turn the sampling delay ON or OFF. This determines whether the auto alignment finds the optimal sampling delay. The default is ON.

Example

:ED:DATA:AAL:CAAL:DEL on

Command

:ED:DATA:AALign:CAALign:DELay?

Description

Return the status of the sampling delay. The returned string is either ON or OFF.

Example

:ED:DATA:AAL:CAAL:DEL?
ON

Command

:ED:DATA:AALign:CAALign:DSTep?

Description

Return the sampling delay step size. The delay step size is fixed at 0.02 UI.

Example

:ED:DATA:AAL:CAAL:DST?
0.002UI

Command

:ED:DATA:AALign:CAALign:SVOLtage

Description

Turn the sampling threshold voltage ON or OFF. This determines whether the auto alignment finds the optimal sampling threshold voltage (eye height). The default is ON. The sampling threshold voltage result will not be available if SVOL is turned OFF.

Example

:ED:DATA:AAL:CAAL:SVOL on

Command

:ED:DATA:AALign:CAALign:SVOLtage?

Description

Return the status of the sampling threshold voltage. The returned string is either ON or OFF.

Example

:ED:DATA:AAL:CAAL:SVOL?
ON

Command

:ED:DATA:AALign:CAALign:SVSTep

Description

Set the sampling threshold voltage step size. The step size is used during an auto alignment in determining the optimal sampling threshold voltage. The optional units are V and mV. The default value/unit is 0.02 V.

Example

:ED:DATA:AAL:CAAL:SVST 20mV

Command

:ED:DATA:AALign:CAALign:SVSTep?

Description

Return the sampling threshold voltage step size. The range is 0.005 V to 0.02 V.

Example

:ED:DATA:AAL:CAAL:SVST?
0.02V

Command

:ED:DATA:AALign:EXECute

Description

Initiate an auto alignment. During an auto alignment the optimal sampling delay and threshold voltage are found.

NOTE Use of auto-align with memory based patterns (.fpt or .usr) is not recommended because it can be quite slow depending on the pattern length. Instead, perform auto-align on a hardware PRBS pattern then switch to the memory based pattern. Changing patterns does not affect alignment.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

```
:ED:DATA:AAL:EXEC;*OPC?
1
```

Command

:ED:DATA:AALign:RESults:EHEight?

Description

Return the eye height after an auto alignment has been performed. The eye height and eye width results are good indicators of the quality of the DUT output.These results are valid to a BER depth of ~1E–6 with a confidence interval of ~95%. They are not intended to be used instead of an eye-mask test, an eye-opening measurement, or TJ measurement. However, the results provide a good first-level indicator of the eye quality.

If an auto alignment has not been performed before initiating this command and the sampling voltage is enabled, N/A will be returned.

Example

:ED:DATA:AAL:RES:EHE?
0.880V

Command

:ED:DATA:AALign:RESults:EWIDth?

Description

Return the eye width after an auto alignment has been performed. The eye height and eye width results are good indicators of the quality of the DUT output.These results are valid to a BER depth of ~1E–6 with a confidence interval of ~95%. They are not intended to be used instead of an eye-mask test, an eye-opening measurement, or TJ measurement. However, the results provide a good first-level indicator of the eye quality.

If an auto alignment has not been performed before initiating this command and delay is enabled, N/A will be returned.

Example

:ED:DATA:AAL:RES:EWID?
0.560UI

Command

:ED:DATA:AALign:RESults:LAALign?

Description

Return the date and time when the last auto alignment was performed.

Example

```
:ED:DATA:AAL:RES:LAAL?
4/07/11       6:03:24
```

Command

:ED:DATA:ACCumulation?

Description

Return the current status of the accumulated BER measurement. The returned string is IDLE, RUNNing, or DONE. After the accumulation is done and the accumulated BER results are cleared, the query result is IDLE.

Example

```
:ED:DATA:ACC?
DONE
```

Command

:ED:DATA:ACCumulation:CLR

Description

Clear the accumulated BER results. This command will only clear results if the accumulated BER measurement is not running.

Example

:ED:DATA:ACC:CLR

Command

:ED:DATA:ACCumulation:RESults:ABER?

Description

Return the accumulated BER results.

NOTE The maximum bit count is approximately 3.4e+38.

Example

:ED:DATA:ACC:RES:ABER?
1.0000e-8

Command

:ED:DATA:ACCumulation:RESults:ALL?

Description

Return the current bit count, error count, accumulated bit error rate, elapsed time, and state (IDLE, RUNNing, or DONE).

NOTE The maximum bit count is approximately 3.4e+38.

Example

:ED:DATA:ACC:RES:ALL?
2.0000e10,0.000e0,0.000e0,10.000S,RUNNING

Command

:ED:DATA:ACCumulation:RESults:BITS?

Description

Return the total accumulated number of bits.

Example

:ED:DATA:ACC:RES:BITS?
9.3000e10

Command

:ED:DATA:ACCumulation:RESults:ELAPsed?

Description

Return the elapsed time since the BER measurement was started.

Example

:ED:DATA:ACC:RES:ELAP?
0000:00:59:10

Command

:ED:DATA:ACCumulation:RESults:ERONes?

Description

Return the accumulated number of 1s resulting in bit errors.

Example

:ED:DATA:ACC:RES:ERON?
5.1500e2

Command

:ED:DATA:ACCumulation:RESults:ERRors?

Description

Return the accumulated number of bit errors.

Example

:ED:DATA:ACC:RES:ERR?
1.0200e3

Command

:ED:DATA:ACCumulation:RESults:ERZeros?

Description

Return the accumulated number of 0s resulting in bit errors.

Example

:ED:DATA:ACC:RES:ERZ?
5.0500e2

Command

:ED:DATA:ACCumulation:SCONfig

Description

Set the stop criteria mode used to define the duration of the measurement. The options are as follows:

MANual
(infinite duration)

DURation
(duration as set by the :ED:DATA:ACCumulation:SCONfig:DURation command)

BITS
(duration determined by total number of accumulated bits as set by the :ED:DATA:ACCumulation:SCONfig:BITS command)

ERRors
(duration determined by total number of accumulated errors as set by the :ED:DATA:ACCumulation:SCONfig:ERRors command)

The default is MANual.

Example

:ED:DATA:ACC:SCON BITS

Command

:ED:DATA:ACCumulation:SCONfig?

Description

Return the current setting of the stop criteria mode used to define the duration of the measurement. The returned string is MANual, DURation, BITS, or ERRors.

Example

:ED:DATA:ACC:SCON?
BITS

Command

:ED:DATA:ACCumulation:SCONfig:BITS

Description

When the stop criteria mode is set to BITS, this command defines the duration of the measurement by the number of accumulated bits. The range is 1e8 through 1e17. The default is 1e9.

Example

:ED:DATA:ACC:SCON:BITS E8

Command

:ED:DATA:ACCumulation:SCONfig:BITS?

Description

Return the number of bits defined for the duration of the measurement. The range is 1e8 through 1e17.

Example

:ED:DATA:ACC:SCON:BITS?
E8

Command

:ED:DATA:ACCumulation:SCONfig:DURation

Description

When the stop criteria mode is set to DURation, this command defines the duration of the measurement in seconds. The range is 1 s through 9999999 s in 1 s increments. The default is 10 s.

Example

:ED:DATA:ACC:SCON:DUR 20s

Command

:ED:DATA:ACCumulation:SCONfig:DURation?

Description

Return the duration in seconds defined for the duration of the measurement. The range is 1 s through 9999999 s.

Example

:ED:DATA:ACC:SCON:DUR?
20.0s

Command

:ED:DATA:ACCumulation:SCONfig:ERRors

Description

When the stop criteria mode is set to ERRors, this command defines the duration of the measurement by the number of accumulated error bits. The range is 1 through 99999999. The default is 1.

Example

:ED:DATA:ACC:SCON:ERR 10

Command

:ED:DATA:ACCumulation:SCONfig:ERRors?

Description

Return the number of accumulated error bits defined for the duration of the measurement. The range is 1 through 99999999.

Example

:ED:DATA:ACC:SCON:ERR?
10

Command

:ED:DATA:ACCumulation:STARt

Description

Start an accumulated BER measurement.

NOTE Starting a BER accumulation does not automatically clear accumulated BER results. Always use the CLR command before starting a BER accumulation to clear results.

Example

:ED:DATA:ACC:CLR
:ED:DATA:ACC:STAR

Command

:ED:DATA:ACCumulation:STOP

Description

Stop an accumulated BER measurement. This command can be issued regardless of the accumulation stop criteria.

Example

:ED:DATA:ACC:STOP

Command

:ED:DATA:INPut:DELay

Description

Set the sampling delay from –2000 UI to 2000 UI in 0.002 UI increments. This sets the amount the clock must be shifted to sample the incoming data to the error detector. In most cases, this value will be centered in the received eye for best performance using auto alignment. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0.00 UI.

The sampling delay can be set manually or automatically by the auto alignment process. See the :ED:DATA:AALign:EXECute command.

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

:ED:DATA:INP:DEL 1000UI;*OPC?
1

Command

:ED:DATA:INPut:DELay?

Description

Return the sampling delay value. The range is –2000 UI to 2000 UI.

Example

:ED:DATA:INP:DEL?
1000UI

Command

:ED:DATA:INPut:IBER?

Description

Return the instantaneous BER. The instantaneous BER is continuously calculated.

Example

:ED:DATA:INP:IBER

Command

:ED:DATA:INPut:SVOLtage

Description

Set the sampling voltage that the error detector uses to sample incoming data from –1.0 V to 1.0 V in 0.001 V increments. The optional units are V and mV. The default value/unit is 0 V.

The sampling voltage can be set manually or automatically by the auto alignment process.

Example

:ED:DATA:INP:SVOL 1V

Command

:ED:DATA:INPut:SVOLtage?

Description

Return the sampling voltage setting. The range is –1.0 V to 1.0 V.

Example

:ED:DATA:INP:SVOL?
1.000V

Command

:ED:DATA:INPut:VTERmination

Description

Set the input termination voltage applied to the inputs of the error detector from –2.0 V to 2.0 V in 0.001 V increments. The optional units are V and mV. The default value/unit is 0 V.

Example

:ED:DATA:INP:VTER 2V

Command

:ED:DATA:INPut:VTERmination?

Description

Return the input termination voltage setting. The range is –2.0 V to 2.0 V.

Example

:ED:DATA:INP:VTER?
2.000V

Command

:ED:DATA:PATTern:APATtern

Description

Turn the auto pattern for PRBS patterns ON or OFF. With auto pattern on, the error detector automatically sets the PRBS pattern and the invert status. The PRBS pattern and the invert status cannot be changed when the auto pattern is on. The default is OFF.

Example

:ED:DATA:PATT:APAT on

Command

:ED:DATA:PATTern:APATtern?

Description

Return the status of the auto pattern for PRBS patterns. The returned string is either ON or OFF.

Example

:ED:DATA:PATT:APAT?
ON

Command

:ED:DATA:PATTern:LIST?

Description

Return the list of all available patterns including factory, PRBS, and user.

Command

:ED:DATA:PATTern:LIST:FACTory?

Description

Return the list of all available factory patterns. These patterns have a filename containing eight characters with a three character extension (.fpt).

Example

:ED:DATA:PATT:LIST:FACTory?
10.FPT, 1100.FPT, 111000.FPT, 11110000.FPT, 81s_80s.FPT, 161_160.FPT, 321_320.FPT, 641_640.FPT, CJPAT.FPT, CJTPAT.FPT, CRPAT.FPT, JSPAT.FPT,
J TSPAT.FPT, K28-3.FPT, K28-5.FPT, K28-7.FPT

Command

:ED:DATA:PATTern:LIST:PRBS?

Description

Return the list of all available PRBS hardware patterns.

Example

:ED:DATA:PATT:LIST:PRBS?
PRBS2^7-1, PRBS2^9-1, PRBS2^10-1, PRBS2^11-1, PRBS2^15-1, PRBS2^23-1, PRBS2^29-1, PRBS2^31-1, PRBS2^33-1, PRBS2^35-1, PRBS2^39-1, PRBS2^41-1, PRBS2^45-1, PRBS2^47-1, PRBS2^49-1, PRBS2^51-1

Command

:ED:DATA:PATTern:LIST:USER?

Description

Return the list of all available user patterns, which are the patterns created via the N4980A multi-instrument BERT software and uploaded to the N4960A serial BERT controller. These patterns have a filename containing eight characters with a three character extension (.usr).

Command

:ED:DATA:PATTern:NAME

Description

Select the data pattern name. The default is PRBS7. The list of PRBS and factory patterns are as follows:

PRBS2^7-1, PRBS2^9-1, PRBS2^10-1, PRBS2^11-1, PRBS2^15-1, PRBS2^23-1, PRBS2^29-1, PRBS2^31-1, PRBS2^33-1, PRBS2^35-1, PRBS2^39-1, PRBS2^41-1, PRBS2^45-1, PRBS2^47-1, PRBS2^49-1, PRBS2^51-1, 10.FPT, 1100.FPT, 111000.FPT, 11110000.FPT, 81s_80s.FPT, 161_160.FPT, 321_320.FPT, 641_640.FPT, CJPAT.FPT, CJTPAT.FPT, CRPAT.FPT, JSPAT.FPT, JTSPAT.FPT, K28-3.FPT, K28-5.FPT, K28-7.FPT

NOTE This command requires some time to execute and the instrument will be unresponsive during this period. Before issuing additional commands, use the *OPC? query command to determine if the operation is complete (indicated by the return of the number “1”). The *OPC? query command can be appended to the command as shown below.

Example

```
:ED:DATA:PATT:NAME PRBS2^7-1;*OPC?
1
```

Command

:ED:DATA:PATTern:NAME?

Description

Return the selected data pattern name.

Example

```
:ED:DATA:PATT:NAME?
PRBS2^7-1
```

Command

:ED:DATA:PATTern:POLarity

Description

Set the data pattern polarity to INVert, to invert the data pattern presented at the data outputs, or NONInvert. The default is NONInvert.

Example

:ED:DATA:PATT:POL INV

Command

:ED:DATA:PATTern:POLarity?

Description

Return the data pattern polarity. The returned string is either INV or NONI.

Example

:ED:DATA:PATT:POL?
INV

Command

:ED:DATA:STATus?

Description

Return the status of the error detector to determine if it is properly aligned. The returned string is OK (decision point is in the optimal position), ALL_ONES (decision point is too low), or ALL_ZEROS (decision point is too high). If all ones or all zeros are detected, the Data Loss LED on the front panel of the error detector turns on.

Example

:ED:DATA:STAT?
OK

Command

:ED:DATA:SYNChronize:EXECute

Description

Initiate a manual synchronization regardless of whether the synchronization mode is set to AUTO or MANual.

Example

:ED:DATA:SYNC:EXEC

Command

:ED:DATA:SYNChronize:MODE

Description

Set the synchronization mode to AUTO or MANual. This specifies whether the error detector will automatically attempt to synchronize to the incoming data stream or will synchronize only when a :ED:DATA:SYNChronize:EXECute command is initiated (MANual).

Example

:ED:DATA:SYNC:MODE AUTO

Command

:ED:DATA:SYNChronize:MODE?

Description

Return the synchronization mode setting. The returned string is either AUTO or MANual.

Example

:ED:DATA:SYNC:MODE?
AUTO

Command

:ED:DATA:SYNChronize:STATus?

Description

Return the synchronization status. The returned string is either SYNC or LOSS. This indicates whether or not the error detector is synchronized to the incoming data stream.

Example

:ED:DATA:SYNC:STAT?
SYNC

Command

:ED:DATA:SYNChronize:STHReshold

Description

Set the synchronization threshold to trigger an automatic synchronization attempt. If the BER rises above this threshold, the error detector will attempt to synchronize if in AUTO mode. An automatic synchronization will not be executed if in MANual mode.

The synchronization threshold rates are as follows:
E-2
E-3
E-4
E-5
E-6
E-7
E-8
E-9

The default is E-2.

Example

:ED:DATA:SYNC:STHR E-3

Command

:ED:DATA:SYNChronize:STHReshold?

Description

Return the synchronization threshold rate. The synchronization threshold rates are as follows:
E-2
E-3
E-4
E-5
E-6
E-7
E-8
E-9

Example

:ED:DATA:SYNC:STHR?
E-3

Command

:ED:DATA:SYNChronize:TYPE?

Description

Return the synchronization type. The default value is NORMal.

Example

:ED:DATA:SYNC:TYPE?
NORM

Command

:ED:DRATe?

Description

Return the current data rate.

Example

:ED:DRATe?
10000000000 bps

6.14 Command Summary

This section provides a summary of SCPI commands for the N4960A serial BERT controller, pattern generator, and error detector.

6.14.1 N4960A Serial BERT Controller Command Summary

The N4960A serial BERT controller device commands are summarized in Table 35.

Table 35. N4960A serial BERT controller command summary

Command	Parameters / Results
:OUTDelay:AMPLitude	*value* <*unit*> ::= 0.3 V to 1.7 V, resolution = 0.005 V
:OUTDelay:AMPLitude?	
:OUTDelay:COUPling	{AC | DC}
:OUTDelay:COUPling?	
:OUTDelay:DELay	*value* <*unit*> ::= –1000 UI to 1000 UI, resolution=.001 UI
:OUTDelay:DELay?	
:OUTDelay:OFFSet	*value* <*unit*> ::= –2.4 V to +2.4 V, resolution = 0.005 V
:OUTDelay:OFFSet?	
:OUTDelay:TERMination	*value* <*unit*> ::= –2.4 V to +2.4 V, resolution = 0.005 V
:OUTDelay:TERMination?	
:OUTDelay:OUTPut	{ON | OFF}
:OUTDelay:OUTPut?	
:OUTJitter:AMPLitude	*value* <*unit*> ::= 0.3 V to 1.7 V, resolution = 0.005 V
:OUTJitter:AMPLitude?	
:OUTJitter:COUPling	{AC | DC}
:OUTJitter:COUPling?	
:OUTJitter:JITTer:EXTernal	{OFF | HIGHband | LOWband}
:OUTJitter:JITTer:EXTernal?	
:OUTJitter:JITTer:EXTernal:LBGain	*value* <*unit*> ::= 0.001 UI/V to 50 UI/V, resolution = 0.001 UI/V
:OUTJitter:JITTer:EXTernal:LBGain?	
:OUTJitter:JITTer:PERiodic	{ON | OFF}

Command	Parameters / Results
:OUTJitter:JITTer:PERiodic?	
:OUTJitter:JITTer:PERiodic:AMPLitude	*value* <*unit*> ::= 0 UI to 100 UI, resolution=0.001 UI
:OUTJitter:JITTer:PERiodic:AMPLitude?	
:OUTJitter:JITTer:PERiodic:FREQuency	*value* <*unit*> ::= 1 Hz to 17 MHz, resolution = 1 Hz
:OUTJitter:JITTer:PERiodic:FREQuency?	
:OUTJitter:JITTer:RANDom	{ON | OFF}
:OUTJitter:JITTer:RANDom?	
:OUTJitter:JITTer:RANDom:AMPLitude	*value* <*unit*> ::= 0 UI to 0.150 UI-rms, resolution=0.001 UI-rms
:OUTJitter:JITTer:RANDom:AMPLitude?	
:OUTJitter:JITTer:SINusoidal1	{ON | OFF}
:OUTJitter:JITTer:SINusoidal1?	
:OUTJitter:JITTer:SINusoidal1:AMPLitude	*value* <*unit*> ::= 0 UI to 1.0 UI, resolution=0.001 UI
:OUTJitter:JITTer:SINusoidal1:AMPLitude?	
:OUTJitter:JITTer:SINusoidal1:FREQuency	*value* <*unit*> ::= 1 Hz to 200 MHz, resolution = 1 Hz
:OUTJitter:JITTer:SINusoidal1:FREQuency?	
:OUTJitter:JITTer:SINusoidal2	{ON | OFF}
:OUTJitter:JITTer:SINusoidal2?	
:OUTJitter:JITTer:SINusoidal2:AMPLitude	*value* <*unit*> ::= 0 UI to 1.0 UI, resolution=0.001 UI
:OUTJitter:JITTer:SINusoidal2:AMPLitude?	
:OUTJitter:JITTer:SINusoidal2:FREQuency	*value* <*unit*> ::= 1 Hz to 200 MHz, resolution = 1 Hz
:OUTJitter:JITTer:SINusoidal2:FREQuency?	
:OUTJitter:OFFSet	*value* <*unit*> ::= –2.4 V to +2.4 V, resolution = 0.005 V
:OUTJitter:OFFSet?	
:OUTJitter:OUTPut	{ON | OFF}
:OUTJitter:OUTPut?	

Command	Parameters / Results
:OUTJitter:TERMination	*value* <*unit*> ::= –2.4 V to +2.4 V, resolution = 0.005 V
:OUTJitter:TERMination?	
:OUTSubrate:AMPLitude	*value* <*unit*> ::= 0.3 V to 1.7 V, resolution = 0.005 V
:OUTSubrate:AMPLitude?	
:OUTSubrate:COUPling	{AC | DC}
:OUTSubrate:COUPling?	
:OUTSubrate:DIVider	*value* ::= 1 to 99999999, resolution = 1
:OUTSubrate:DIVider?	
:OUTSubrate:OFFSet	*value* <*unit*> ::= –2.4 V to +2.4 V, resolution = 0.005 V
:OUTSubrate:OFFSet?	
:OUTSubrate:OUTPut	{ON | OFF}
:OUTSubrate:OUTPut?	
:OUTSubrate:TERMination	*value* <*unit*> ::= –2.4 V to +2.4 V, resolution = 0.005 V
:OUTSubrate:TERMination?	
:SOURce:DCLock:FREQuency	*value* <*unit*> ::= 1 to 16 GHz, resolution = 1 kHz
:SOURce:DCLock:FREQuency?	
:SOURce:DCLock:PATH	{SYSTem | EXTernal}
:SOURce:DCLock:PATH?	
:SOURce:FREQuency	*value* <*unit*> ::= 1 to 16 GHz, resolution = 1 kHz
:SOURce:FREQuency?	
:SOURce:FREQuency:CW	*value* <*unit*> ::= 1 to 16 GHz, resolution = 1 kHz
:SOURce:FREQuency:CW?	
:SOURce:FREQuency:PATH	{INTernal | EXTernal}
:SOURce:FREQuency:PATH?	
:SOURce:ROSCillator:PATH	{AUTO | INTernal | EXTernal}
:SOURce:ROSCillator:PATH?	
:SOURce:SSCLocking	{ON | OFF}
:SOURce:SSCLocking?	
:SOURce:SSCLocking:DEViation	*value* <*unit*> ::= 0 PPM to 10000 PPM, resolution = 1 PPM

Command	Parameters / Results
:SOURce:SSCLocking:DEViation?	
:SOURce:SSCLocking:FREQuency	*value* <*unit*> ::= 1 Hz to 50000 Hz, resolution = 1 Hz
:SOURce:SSCLocking:FREQuency?	
:SOURce:SSCLocking:TYPE	{DOWN | UP | CENTer}
:SOURce:SSCLocking:TYPE?	
:SYSTem:DATE	Sets the current date
:SYSTem:DATE?	Responds with current date
:SYSTem:ERRor?	Responds with the oldest Event/Error log report.
:SYSTem:ERRor:ALL?	Responds with all Event/Error log reports.
:SYSTem:ERRor:COUNt?	Queries the error/event queue for the number of unread items.
:SYSTem:ERRor:NEXT?	Gives the next Event/Error log report.
:SYSTem:HEADs?	Responds with currently connected remote heads including type, hardware version, firmware version, and serial number.
:SYSTem:LLOCkout	Local lockout (panel locked out)
:SYSTem:LOCal	Places instrument in local mode.
:SYSTem:PRESet	Execute a system preset.
:SYSTem:STATe:RECall	Recall a previously stored state.
:SYSTem:STATe:SAVE	Save a system state.
:SYSTem:TIME?	Responds with current time.
:SYSTem:TIME	Set the current time.
:SYSTem:VERSion?	Responds with current version of SCPI commands.

6.14.2 Pattern Generator Command Summary

The pattern generator device commands are summarized in Table 36.

Table 36. Pattern generator command summary

Command	Parameters / Results
:PG:DATA:DEEMphasis:POST1	value <unit> ::= 0 to –30 dB resolution=0.1 dB
:PG:DATA:DEEMphasis:POST1?	
:PG:DATA:DEEMphasis:POST2	value <unit> ::= –30 to +30 dB resolution=0.1 dB
:PG:DATA:DEEMphasis:POST2?	
:PG:DATA:DEEMphasis:POST3	value <unit> ::= –30 to +30 dB resolution=0.1 dB
:PG:DATA:DEEMphasis:POST3?	
:PG:DATA:DEEMphasis:PRECursor	value <unit> ::= 0 to +30 dB resolution=0.1 dB
:PG:DATA:DEEMphasis:PRECursor?	
:PG:DATA:LLEVel	{LVPECL | LVDS | ECL | CUSTom}
:PG:DATA:LLEVel?	
:PG:DATA:LLEVel:AMPLitude	N4951A-P17/-P32 (only) *value* <*unit*> ::= 0.1 V (p-p) to 1.0 V (p-p), resolution = 0.005 V N4951B-H17/-H32 (only) *value* <*unit*> ::= 0.3 V (p-p) to 3.0 V (p-p), resolution = 0.005 V N4951B-D17/-D32 (only) *value* <*unit*> ::= 0.3 V (p-p) to 1.5 V (p-p), resolution = 0.005 V
:PG:DATA:LLEVel:AMPLitude?	
:PG:DATA:LLEVel:OFFSet	*value* <*unit*> ::= –2.0 V to +2.0 V, resolution = 0.005 V
:PG:DATA:LLEVel:OFFSet?	
:PG:DATA:LLEVel:TERMination	*value* <*unit*> ::= –2.0 V to +2.0 V, resolution = 0.005 V
:PG:DATA:LLEVel:TERMination?	
:PG:DATA:OUTPut	{ON | OFF}
:PG:DATA:OUTPut?	
:PG:DATA:OUTPut:DELay	*value* <*unit*> ::= –2000 UI to 2000 UI, resolution = 0.002 UI (applies to channel 1 only)

Command	Parameters / Results
:PG:DATA:OUTPut:DELay?	(applies to channel 1 only)
:PG:DATA:PATTern:ERRInjection	{ON | OFF}
:PG:DATA:PATTern:ERRInjection?	
:PG:DATA:PATTern:ERRInjection:RATE	{E-3 | E-4 | E-5 | E-6 | E-7 | E-8 | E-9}
:PG:DATA:PATTern:ERRInjection:RATE?	
:PG:DATA:PATTern:ERRInjection:SINGle	Momentary command to inject a single error then turns off
:PG:DATA:PATTern:LIST?	Responds with the list of all patterns
:PG:DATA:PATTern:LIST:FACTory?	Responds with the list of factory patterns
:PG:DATA:PATTern:LIST:PRBS?	Responds with the list of PRBS hardware patterns
:PG:DATA:PATTern:LIST:USER?	Responds with the list of user patterns
:PG:DATA:PATTern:NAME	{PRBS2^7-1 | PRBS2^9-1 | PRBS2^10-1 | PRBS2^11-1 | PRBS2^15-1 | PRBS2^23-1 | PRBS2^29-1 | PRBS2^31-1 | PRBS2^33-1 | PRBS2^35-1 | PRBS2^39-1 | PRBS2^41-1 | PRBS2^45-1 | PRBS2^47-1 | PRBS2^49-1 | PRBS2^51-1 | 10.FPT | 1100.FPT | 111000.FPT | 11110000.FPT | 81s_80s.FPT | 161_160.FPT | 321_320.FPT | 641_640.FPT |CJPAT.FPT | CJTPAT.FPT | CRPAT.FPT | JSPAT.FPT | JTSPAT.FPT | K28-3.FPT | K28-5.FPT |K28-7.FPT }
:PG:DATA:PATTern:NAME?	
:PG:DATA:PATTern:POLarity	{INVert | NONInvert}
:PG:DATA:PATTern:POLarity?	
:PG:DATA:XOVer	*value* <*unit*> ::= 25% to 75%, resolution = 1%
:PG:DATA:XOVer?	
:PG:DRATe?	Responds with the current data rate (two times the clock frequency)

6.14.3 Error Detector Command Summary

The error detector device commands are summarized in Table 37.

Table 37. Error detector command summary

Command	Parameters / Results
:ED:DATA:AALign:CAALign:DELay	{ON | OFF}
:ED:DATA:AALign:CAALign:DELay?	
:ED:DATA:AALign:CAALign:DSTep?	
:ED:DATA:AALign:CAALign:SVOLtage	{ON | OFF}
:ED:DATA:AALign:CAALign:SVOLtage?	
:ED:DATA:AALign:CAALign:SVSTep	*value* <*unit*> ::= 0.005 V to 0.020 V, resolution = 0.001 V
:ED:DATA:AALign:CAALign:SVSTep?	
:ED:DATA:AALign:EXECute	Momentary command to initiate an auto align
:ED:DATA:AALign:RESults:EHEight?	Responds with the eye height
:ED:DATA:AALign:RESults:EWIDth?	Responds with the eye width
:ED:DATA:AALign:RESults:LAALign?	Responds with the date/time of the last auto align
:ED:DATA:ACCumulation:CLR	Momentary command to clear the results of an accumulated BER measurement
:ED:DATA:ACCumulation:RESults:ABER?	Responds with the accumulated BER results
:ED:DATA:ACCumulation:RESults:ALL?	Responds with the current bit count, error count, accumulated BER, elapsed time, and state
:ED:DATA:ACCumulation:RESults:BITS?	Responds with the accumulated number of bits
:ED:DATA:ACCumulation:RESults:ELAPsed?	Responds with the elapsed time of the measurement
:ED:DATA:ACCumulation:RESults:ERONes?	Responds with the accumulated number of 1s resulting in a bit error
:ED:DATA:ACCumulation:RESults:ERRors?	Responds with the accumulated number of errors
:ED:DATA:ACCumulation:RESults:ERZeros?	Responds with the accumulated number of 0s resulting in a bit error
:ED:DATA:ACCumulation:SCONfig	{MANual | DURation | BITS | ERRors}
:ED:DATA:ACCumulation:SCONfig?	
:ED:DATA:ACCumulation:SCONfig:BITS	{E8 | E9 | E10 | E11 | E12 | E13 | E14 | E15 | E16 | E17}
:ED:DATA:ACCumulation:SCONfig:BITS?	
:ED:DATA:ACCumulation:SCONfig:DUR	*value* <*unit*> ::= 1 s to 9999999 s, resolution = 1 s
:ED:DATA:ACCumulation:SCONfig:DUR?	
:ED:DATA:ACCumulation:SCONfig:ERRors	*value* ::= 1 to 99999999, resolution = 1

Command	Parameters / Results
:ED:DATA:ACCumulation:SCONfig:ERRors?	
:ED:DATA:ACCumulation:STARt	Momentary command to initiate an accumulated BER measurement
:ED:DATA:ACCumulation:STOP	Momentary command to stop an accumulated BER measurement
:ED:DATA:ACCumulation?	Responds with the status of the accumulated BER: [IDLE | RUNNing | DONE]
:ED:DATA:INPut:DELay	*value* <*unit*> ::= –2000 UI to 2000 UI, resolution = 0.002 UI
:ED:DATA:INPut:DELay?	
:ED:DATA:INPut:IBER?	Responds with the instantaneous BER
:ED:DATA:INPut:SVOLtage	*value* <*unit*> ::= –1.0 V to +1.0 V, resolution = 0.001 V
:ED:DATA:INPut:SVOLtage?	
:ED:DATA:INPut:VTERmination	*value* <*unit*> ::= –2.0 V to +2.0 V, resolution = 0.001 V
:ED:DATA:INPut:VTERmination?	
:ED:DATA:PATTern:APATtern	{ON | OFF}
:ED:DATA:PATTern:APATtern?	
:ED:DATA:PATTern:LIST:FACTory?	Responds with the list of factory patterns
:ED:DATA:PATTern:LIST:PRBS?	Responds with the list of PRBS hardware patterns
:ED:DATA:PATTern:LIST:USER?	Responds with the list of user patterns
:ED:DATA:PATTern:NAME	{PRBS2^7-1 | PRBS2^9-1 | PRBS2^10-1 | PRBS2^11-1 | PRBS2^15-1 | PRBS2^23-1 | PRBS2^29-1 | PRBS2^31-1 | PRBS2^33-1 | PRBS2^35-1 | PRBS2^39-1 | PRBS2^41-1 | PRBS2^45-1 | PRBS2^47-1 | PRBS2^49-1 | PRBS2^51-1 | 10.FPT | 1100.FPT | 111000.FPT | 11110000.FPT | 81s_80s.FPT | 161_160.FPT | 321_320.FPT | 641_640.FPT |CJPAT.FPT | CJTPAT.FPT | CRPAT.FPT | JSPAT.FPT | JTSPAT.FPT | K28-3.FPT | K28-5.FPT |K28-7.FPT }
:ED:DATA:PATTern:NAME?	
:ED:DATA:PATTern:POLarity	{INVert | NONInvert}
:ED:DATA:PATTern:POLarity?	
:ED:DATA:STATus?	Responds with the status of the error detector alignment: [OK | ALL_ONES | ALL_ZEROS]
:ED:DATA:SYNChronize:EXECute	Momentary command to perform a manual synchronization

Command	Parameters / Results
:ED:DATA:SYNChronize:MODE	{AUTO | MANual}
:ED:DATA:SYNChronize:MODE?	
:ED:DATA:SYNChronize:STATus?	{SYNC | LOSS}
:ED:DATA:SYNChronize:STHReshold	{E-2 | E-3 | E-4 | E-5 | E-6 | E-7 | E-8 | E-9}
:ED:DATA:SYNChronize:STHReshold?	
:ED:DATA:SYNChronize:TYPE?	NORMal
:ED:DRATe?	Responds with the current data rate (two times the clock frequency)

6.15 Programming Example

The following programming example is written in Python, an open-source programming language that is free to use, even for commercial products. The open-source PyVISA package enables fast and easy GPIB and USB instrument control.

The example program below demonstrates some popular methods of interfacing with the N4960A serial BERT 17 and 32 Gb/s. The program was written for a 32 Gb/s system. Contact support@Keysight Technologies.com if you have any additional questions or if you would like help programming our instruments.

```
# use the PyVISA plugin from http://pyvisa.sourceforge.net/
import visa
import time

def pause():
   print 'press return to continue'
   cont=raw_input()

# instrument setup, change addresses to suit your equipment
address = "ASRL46" # e.g. "GPIB::18" for GPIB address 18, "ASRL15" for COM15
#                (FTDI driver enables COM over USB)
timeout = 1000     # default 1s timeout for queries
resetN4960A = True   # option to reset the instrument when starting

# connect to instrument and turn off local echo if using USB
# -local echo may be on or off, which means the !ECHO OFF
#   command may be repeated back to us, this is tricky
print "connecting to " + address
N4960A = visa.instrument(address)
N4960A.clear
if (address.find("ASRL") != -1):

   N4960A.write("!ECHO OFF")
   N4960A.timeout = 1
   try:
      tmp = N4960A.read()
   except:
      N4960A.clear
   N4960A.timeout = timeout

# clear errors
null = N4960A.ask("*ESR?").strip("\n")
null = N4960A.ask(":SYST:ERR:ALL?").strip("\n")

# query instrument type
```

```
idn = N4960A.ask("*IDN?").strip("\n")
idnManufacturer, idnModel, idnSN, idnRev = idn.split(",")
idnModel = idnModel.upper().strip(" ")
idnSN = idnSN.strip(" ").lstrip("0")
if idnModel.find("N4960-CJ0") != -1:
   print "found " + idnModel + " serial number " + idnSN,
   if idnModel.find("J") != -1:
      N4960AJitter = True
      print "(with jitter)"
   else:
      N4960AJitter = False
      print "(without jitter)"
else:
   print "unrecognized instrument: " + idn
   exit

# query remote heads
heads = N4960A.ask(":SYST:HEAD?").strip("\n").strip("\r")
pg,ed,null = heads.split(":")
pgType,pgSN,pgHW,pgFW = pg.split(",")
if pgType.find("P32 ") != -1:
   P32  = True
   print "found head: " + pgType + " serial number " + pgSN
edType,edSN,edHW,edFW = ed.split(",")
if edType.find("E32 ") != -1:
   E32  = True
   print "found head: " + edType + " serial number " + edSN

# reset the instrument, if desired
if resetN4960A:
   print "resetting instrument:",
   N4960A.write("*RST")
   N4960A.write("*OPC?")
   print "done"
```

```
# clear any errors from the queue
def errchk():
   print "error queue:",
   esr = int(N4960A.ask("*ESR?").strip("\n"))
   if (esr != 0): print "*ESR? error #%d" % esr
   print N4960A.ask(":SYST:ERR:ALL?").strip("\n")

# next section
errchk()
print ""
# turn on internal clock and set frequency to 7.0125GHz (equiv to 14.025Gb/s)
print "setting clock:",
N4960A.write(":SOUR:FREQ:PATH INT; *OPC?")
print N4960A.ask(":SOUR:FREQ:PATH?").strip("\n"),
N4960A.write(":SOUR:FREQ %.3fGHz; *OPC?" % 7.0125)
print N4960A.ask(":SOUR:FREQ?").strip("\n")

# set delayed N4960A clock outputs on, to 1Vpp and 0.5UI delay
print "delayed clock outputs:",
N4960A.write(":OUTD:AMPL 1V")
print N4960A.ask(":OUTD:AMPL?").strip("\n"),

N4960A.write(":OUTD:OUTP ON")
print N4960A.ask(":OUTD:OUTP?").strip("\n"),
N4960A.write(":OUTD:DEL 0.5UI; *OPC?")
print N4960A.ask(":OUTD:DEL?").strip("\n")

# set divided N4960A clock outputs on, to 1Vpp and div/64 rate
print "divided clock outputs:",
N4960A.write(":OUTS:AMPL 1V")
print N4960A.ask(":OUTS:AMPL?").strip("\n"),
N4960A.write(":OUTS:DIV 64")
print N4960A.ask(":OUTS:DIV?").strip("\n"),
N4960A.write(":OUTS:OUTP ON")
print N4960A.ask(":OUTS:OUTP?").strip("\n")
```

```
# next section
errchk()
print ""
# if jitter option enabled, apply some!
if N4960AJitter:
   # set jittered N4960A clock outputs on, to 1Vpp
   print "jittered outputs:",
   N4960A.write(":OUTJ:AMPL 1V")
   print N4960A.ask(":OUTJ:AMPL?").strip("\n"),
   N4960A.write(":OUTJ:OUTP ON")
   print N4960A.ask(":OUTJ:OUTP?").strip("\n")

   # turn on SSC: 33kHz 0/-0.5%
   print "SSC:",

   N4960A.write(":SOUR:SSCL ON; *OPC?")
   print N4960A.ask(":SOUR:SSCL?").strip("\n"),
   N4960A.write(":SOUR:SSCL:FREQ 33kHz")
   print N4960A.ask(":SOUR:SSCL:FREQ?").strip("\n"),
   N4960A.write(":SOUR:SSCL:DEV 0.5pct")
   print N4960A.ask(":SOUR:SSCL:DEV?").strip("\n"),
   N4960A.write(":SOUR:SSCL:TYP DOWN")
   print N4960A.ask(":SOUR:SSCL:TYP?").strip("\n"),
   print "SSC ON, 33kHz -0.5%"

   # turn off SSC
   print "SSC:",
   N4960A.write(":SOUR:SSCL OFF; *OPC?")
   print N4960A.ask(":SOUR:SSCL?").strip("\n")

   # turn off SJ1, SJ2, RJ
   print "Jitter:",
   N4960A.write(":OUTJ:JITT:PER OFF;*OPC?")
   print "PJ:",
   opc = N4960A.ask("*OPC?")
   print N4960A.ask(":OUTJ:JITT:PER?").strip("\n"),
   N4960A.write(":OUTJ:JITT:SIN1 OFF")
   print "SJ1:",
   print N4960A.ask(":OUTJ:JITT:SIN1?").strip("\n"),
   N4960A.write(":OUTJ:JITT:SIN2 OFF")
   print "SJ2:",
   print N4960A.ask(":OUTJ:JITT:SIN2?").strip("\n"),
   N4960A.write(":OUTJ:JITT:RAND OFF")
   print "RJ:",
   print N4960A.ask(":OUTJ:JITT:RAND?").strip("\n")

   # turn on PJ and adjust to 0.32UI at 2.4MHz
```

```
# NOTE all jitter amplitudes are for the Jittered Clock outputs
# and the jitter ampitude is doubled (x2) for the PG17/32 outputs
# i.e. 0.32UI PJ for the jittered clock output provides 0.64UI at the PG head
print "PJ:",
N4960A.write(":OUTJ:JITT:PER ON; *OPC?")
print N4960A.ask(":OUTJ:JITT:PER?").strip("\n"),
N4960A.write(":OUTJ:JITT:PER:FREQ 2.4MHz")
print N4960A.ask(":OUTJ:JITT:PER:FREQ?").strip("\n").strip(" "),
N4960A.write(":OUTJ:JITT:PER:AMPL 0.32UI; *OPC?")
print N4960A.ask(":OUTJ:JITT:PER:AMPL?").strip("\n")

# turn off PJ
print "PJ:",
N4960A.write(":OUTJ:JITT:PER OFF; *OPC?")
print N4960A.ask(":OUTJ:JITT:PER?").strip("\n")

# turn on SJ1 and adjust to 0.25UI at 100MHz
print "SJ1:",
N4960A.write(":OUTJ:JITT:SIN1 ON")
N4960A.write(":OUTJ:JITT:SIN1:FREQ 100MHz")
print N4960A.ask(":OUTJ:JITT:SIN1:FREQ?").strip("\n").strip(" "),
N4960A.write(":OUTJ:JITT:SIN1:AMPL 0.25UI")
print N4960A.ask(":OUTJ:JITT:SIN1:AMPL?").strip("\n")

# turn on SJ2 and adjust to 0.15UI at 150MHz
print "SJ2:",
N4960A.write(":OUTJ:JITT:SIN2 ON")
N4960A.write(":OUTJ:JITT:SIN2:FREQ 150MHz")
print N4960A.ask(":OUTJ:JITT:SIN2:FREQ?").strip("\n").strip(" "),
N4960A.write(":OUTJ:JITT:SIN2:AMPL 0.15UI")
print N4960A.ask(":OUTJ:JITT:SIN2:AMPL?").strip("\n")

# turn on RJ and adjust to 0.02UI rms
print "RJ:",
N4960A.write(":OUTJ:JITT:RAND ON")
print N4960A.ask(":OUTJ:JITT:RAND?").strip("\n"),
N4960A.write(":OUTJ:JITT:RAND:AMPL 0.02")
print N4960A.ask(":OUTJ:JITT:RAND:AMPL?").strip("\n")
```

```
# turn off SJ1, SJ2, RJ
print "Jitter:",
N4960A.write(":OUTJ:JITT:PER OFF;*OPC?")
print "PJ:",
opc = N4960A.ask("*OPC?")
print N4960A.ask(":OUTJ:JITT:PER?").strip("\n"),
N4960A.write(":OUTJ:JITT:SIN1 OFF")
print "SJ1:",
print N4960A.ask(":OUTJ:JITT:SIN1?").strip("\n"),
N4960A.write(":OUTJ:JITT:SIN2 OFF")
print "SJ2:",
print N4960A.ask(":OUTJ:JITT:SIN2?").strip("\n"),
N4960A.write(":OUTJ:JITT:RAND OFF")
print "RJ:",
print N4960A.ask(":OUTJ:JITT:RAND?").strip("\n")

# next section
errchk()
print ""

# if a PG head is attached, lets control it!
if P32 :
# set amplitude and turn the output on, 0.5Vpp
print pgType + ":",
   print N4960A.ask(":PG:DRAT?").strip("\n"),
   N4960A.write(":PG :DATA:LLEV:AMPL 0.5")
   print N4960A.ask(":PG:DATA:LLEV:AMPL?").strip("\n"),
   N4960A.write(":PG :DATA:OUTP ON")
   print N4960A.ask(":PG:DATA:OUTP?").strip("\n"),

   # set the pattern to PRBS9, non-inverted, no error injection
   # this could take a while for user patterns
   N4960A.write(":PG:DATA:PATT:NAME PRBS2^9-1; *OPC?")
   print N4960A.ask(":PG:DATA:PATT:NAME?").strip("\n"),
   N4960A.write(":PG:DATA:PATT:POL NONI")
   print N4960A.ask(":PG:DATA:PATT:POL?").strip("\n"),
   N4960A.write(":PG:DATA:PATT:ERRI OFF")
   print "error inject:",
   print N4960A.ask(":PG:DATA:PATT:ERRI?").strip("\n")
```

```
    # next section
    errchk()
    print ""

# if an ED head is attached, lets control it!
if E32 :
    # set sampling threshold to 0V, data delay to 0UI
    print edType + ":",
    print N4960A.ask(":ED:DRAT?").strip("\n"),
    N4960A.write(":ED:DATA:INP:SVOL 0")
    print "0/1 thr:",
    print N4960A.ask(":ED:DATA:INP:SVOL?").strip("\n"),
    N4960A.write(":ED:DATA:INP:DEL 0")
    print "data delay:",
    print N4960A.ask(":ED:DATA:INP:DEL?").strip("\n"),

    # set the pattern to PRBS9, non-inverted
    # this could take a while for user patterns
    N4960A.write(":ED:DATA:PATT:NAME PRBS2^9-1; *OPC?")
    print N4960A.ask(":ED:DATA:PATT:NAME?").strip("\n"),
    N4960A.write(":ED:DATA:PATT:POL NONI")
    print N4960A.ask(":ED:DATA:PATT:POL?").strip("\n")

    # indicate if there's data detected
    dataDetected = N4960A.ask(":ED:DATA:STAT?").strip("\n")
    print "input data: " + dataDetected
    if dataDetected.find("OK") != -1:
        # lets try to auto-align (time and voltage) and check sync
        print "auto-align:",
N4960A.write(":ED:DATA:AAL:CAAL:SVOL ON") # include 0/1 threshold voltage sweep

        #                               auto-align routine
        print "Threshold:",
        print N4960A.ask(":ED:DATA:AAL:CAAL:SVOL?").strip("\n"),
N4960A.write(":ED:DATA:AAL:CAAL:DEL ON") # include data delay sweep in
        #                               auto-align routine
        print "Data delay",
        print N4960A.ask(":ED:DATA:AAL:CAAL:DEL?").strip("\n"),
        print "executing.. please wait..",
        N4960A.write(":ED:DATA:AAL:EXEC; *OPC?")
        # this could take a while
        print "..done"
        print "Auto-align result: 0/1 Threshold =",
        print N4960A.ask(":ED:DATA:AAL:RES:EHE?").strip("\n"),
        print ",  Data delay =",
        print N4960A.ask(":ED:DATA:AAL:RES:EWID?").strip("\n")
        print "Eye height =",
```

```
print N4960A.ask(":ED:DATA:AAL:RES:EHE?").strip("\n"),
print ",  Eye width =",
print N4960A.ask(":ED:DATA:AAL:RES:EWID?").strip("\n")

# check the sync status
syncStatus = N4960A.ask(":ED:DATA:SYNC:STAT?").strip("\n")
print "sync: " + syncStatus
time.sleep(1)
syncStatus = N4960A.ask(":ED:DATA:SYNC:STAT?").strip("\n")
print "sync: " + syncStatus
if syncStatus.find("SYNC") != -1:
   # lets try to make a BER measurement
   print "measuring BER"
   # check to see if we are running measurement
   measStatus = N4960A.ask(":ED:DATA:ACC?").strip("\n")
   print "Accumulation status is " + measStatus
   # if running, stop accumulation
   if measStatus.find("IDLE") != -1:
      N4960A.write(":ED:DATA:ACC:STOP")
   else:
      if measStatus.find("DONE") != -1:
         N4960A.write(":ED:DATA:ACC:STOP")
   measStatus = N4960A.ask(":ED:DATA:ACC?").strip("\n")
   print "Accumulation status is " + measStatus
   # clear previous accumulation results
   N4960A.write(":ED:DATA:ACC:CLR")
   print "Bits       = " + N4960A.ask(":ED:DATA:ACC:RES:BITS?").strip("\n")
   # set accumulation time to 10 seconds
   N4960A.write(":ED:DATA:ACC:SCON DUR")
   N4960A.write(":ED:DATA:ACC:SCON:DUR 10")
   # start the measurement
   N4960A.write(":ED:DATA:ACC:STAR")
   print "Accumulation status is " + N4960A.ask(":ED:DATA:ACC?").strip("\n")
   # while loop to read results once per second
   t=0
   time.sleep(1)
   while t<11:
      t=t+1
      print t, N4960A.ask(":ED:DATA:INP:IBER?").strip("\n")
      time.sleep(1)
   print "Accumulation status is " + N4960A.ask(":ED:DATA:ACC?").strip("\n")
   print "Accumulation results: "
   print "BER        = " + N4960A.ask(":ED:DATA:ACC:RES:ABER?").strip("\n")
   print "Time       = " + N4960A.ask(":ED:DATA:ACC:RES:ELAP?").strip("\n")
   print "Bits       = " + N4960A.ask(":ED:DATA:ACC:RES:BITS?").strip("\n")
   print "Errors     = " + N4960A.ask(":ED:DATA:ACC:RES:ERR?").strip("\n")
   print "Errored 1's = " + N4960A.ask(":ED:DATA:ACC:RES:ERON?").strip("\n")
   print "Errored 0's = " + N4960A.ask(":ED:DATA:ACC:RES:ERZ?").strip("\n")
```

```
    else:
        print "** no pattern synchronization, cannot make measurement"
else:
    print "** no data input detected, cannot make measurement"

# next section
errchk()
print ""
```

The program above generates the following output:

```
connecting to ASRL46
found N4960A-CJ1 serial number 309 (with jitter)
found head: P32 serial number 03.00
found head: E32 serial number 02.00
resetting instrument: done
error queue: 0, "No error"

setting clock: INT 7013000000 Hz
delayed clock outputs: 1.000V ON 0.50UI
divided clock outputs: 1.000V 64 ON
error queue: 0, "No error"

jittered outputs: 1.000V ON
SSC: ON 33000 Hz 5000PPM DOWN SSC ON, 33kHz -0.5%
SSC: OFF
Jitter: PJ: OFF SJ1: OFF SJ2: OFF RJ: OFF
PJ: ON 2400000 Hz 0.320UI
PJ: OFF
SJ1: 200000000 Hz 0.250UI
SJ2: 150000000 Hz 0.150UI
RJ: ON 0.050UI-rms
Jitter: PJ: OFF SJ1: OFF SJ2: OFF RJ: OFF
error queue: 0, "No error"

P32 : 14026000000 bps 0.500V ON PRBS2^9-1 NONI error inject: OFF
error queue: 0, "No error"


E32 : 14026000000 bps 0/1 thr: 0.000V data delay: +0.00UI PRBS2^9-1 NONI
input data: OK
auto-align: Threshold: ON Data delay ON executing.. please wait.. ..done
Auto-align result: 0/1 Threshold =  0.340V ,  Data delay =  0.840UI
Eye height =  0.340V ,  Eye width =  0.840UI
sync: SYNC
sync: SYNC
measuring BER
Accumulation status is IDLE
Accumulation status is IDLE
```

```
Bits        = +0.0000e0
Accumulation status is RUNN
1 +0.000000e0
2 +0.000000e0
3 +0.000000e0
4 +0.000000e0
5 +0.000000e0
6 +0.000000e0
7 +0.000000e0
8 +0.000000e0
9 +0.000000e0
10 +0.000000e0
11 +0.000000e0
Accumulation status is IDLE
Accumulation results:
BER         = 0.0000e0
Time        =  0000:00:00:10
Bits        = +1.4307e11
Errors      = +0.0000e0
Errored 1's = +0.0000e0
Errored 0's = +0.0000e0
error queue: 0, "No error"
```

6.16 Programming Tips

Some commands to control the N4960A serial BERT 17 and 32 Gb/s may take a long time to execute completely. These are listed in Table 38.

Table 38. N4960A serial BERT commands that should be accompanied by *OPC? or *WAI

Command
:SOURce:FREQuency
:SOURce:FREQuency:CW
:SOURce:FREQuency:PATH
:OUTJitter:JITTer:PERiodic
:OUTJitter:JITTer:PERiodic:AMPLitude
:OUTJitter:JITTer:EXTernal
:OUTJitter:JITTer:EXTernal:LBGain
:OUTDelay:DELay and :ED:DATA:INPut:DELay
:SYSTem:PRESet
:PG:DATA:PATTern:NAME and :ED:DATA:PATTern:NAME
:ED:DATA:AALign:EXECute
*RCL
*RST (*OPC? cannot be appended to this command. It must be issued as a separate query.)

In order to avoid issues when programming with these commands, such as bus timeout, the use of IEEE 488.2 commands *OPC? (Operation Complete Query) or *WAI (Wait to Continue) should be used. For example, a large change to the precision delay (using the :OUTDelay:DELay command) can take many seconds to complete, and the controlling program may want subsequent commands to wait until it has completed before proceeding.

With either solution, the bus timeout needs to be set appropriately. Timing for some N4960A commands can be found in Section 6.17.4.

NOTE The *OPC and *OPC? commands must be the last commands on a line. The *WAI and *ESR? commands do not have to be the last commands on a line.

6.16.1 Example Using *OPC?

The *OPC? query should be used to synchronize the host computer with the instrument. The *OPC? query does not return until the previous operation has been completed, thus allowing synchronization between the controlling program and instrument. Used in the example below, it causes the controlling program to wait until the delay setting command is complete before attempting to enable the Delayed Clock outputs. If the *OPC? query is not included after commands that may take a while to complete, then commands or queries issued ***after*** those commands may timeout.

```
N4960A.write(":SOUR:FREQ %.3fGHz; *OPC?" % 7.0125)
print N4960A.ask(":SOUR:FREQ?").strip("\n")
```

NOTE

Do not use the *OPC? command on the same line as the *RST command (for example, "*RST;*OPC?"). The *RST command should only be issued as a stand-alone command. To ensure that the instrument is ready to use after issuing the *RST command, perform a query (write/read) on the command "*OPC?". When *OPC returns, the instrument is ready to use, no wait or sleep commands are necessary.

6.16.2 Example Using *WAI

Alternatively, the *WAI command should be used to synchronize commands contained in a single line; it synchronizes the commands inside the instrument. *WAI prevents the instrument from processing further commands or queries until all pending operations are complete. The commands below accomplish the same objective as the previous example. The first command will be executed, the *WAI will delay until the command has been completed, and then the final command will be executed.

```
N4960A.write(":OUTD:DEL 0.5UI; *WAI; :OUTD:OUTP ON")
```

6.16.3 Communication Timeouts

Most SCPI commands of the N4960A serial BERT 17 and 32 Gb/s are processed quickly and return within milliseconds. A few commands require a longer time to take place and process.

The user should use “*OPC?” or “*WAI” after the SCPI command or “*OPC” followed by “*ESR?” for the commands listed in Table 38.

Furthermore, the bus interface timeout needs to be set to two minutes, or 120,000 ms, to ensure that all commands can complete without triggering the communication timeout for the following cases:

1. Large delay change

   Example: Set the delay of the delay outputs from the default state (0 UI) to 1000 UI.

   :OUTD:DEL 1000; *OPC?

   It will take approximately 17 seconds to set the delay from 0 UI to 1000 UI or from -1000 UI to 0 UI.

2. System Preset

   :SYST:PRES; *WAI

   This command will put the N4960A serial BERT 17 and 32 Gb/s back into the default state. It will take approximately 9 seconds.

   However, if the System Preset command is issued from a state of the instrument which has very large amount of delay as mentioned above, an additional time needed to set the delay back to 0 UI should be added on top of the 9 seconds.

   For example: If the present instrument state has the delay set to 1000 UI. The command “:SYST:PRES; *WAI” will complete after 26 seconds.

3. Recall

   *RCL [x]

   *OPC?

   This command recalls the instrument’s state from the register x (x = 1 to 5). It takes less than a second to complete. However, if the recalled state includes a large delay change as mentioned above, an additional time should be added in order to complete the task.

4. Frequency source setting

   :SOUR:FREQ:PATH [INT|EXT]; *OPC?

   A valid external clock should be applied at EXT CLK INPUT of the instrument before switching from internal to external state. If there is no valid external clock input applied, it will take approximately 6 seconds to complete the switching from External to Internal state.

5. External Jitter

   A valid external signal should be applied at the EXT JITTER INPUT of the instrument before switching from OFF to LOW or HIGH.

   In the case when no valid external signal is applied:

6. It will take approximately 15 seconds to complete the switching from OFF or Highband to Lowband state with command: ":OUTJ:JITT:EXT LOW; *WAI".
7. It will take approximately 5 seconds to set a Lowband Gain value with command: ":OUTJ:JITT:EXT:LBG xx; *WAI".
8. It will take approximately 6 seconds to complete to switch from Lowband to Highband state with command: ":OUTJ:JITT:EXT HIGH; *WAI".
9. Periodic Jitter Amplitude

   Example: Set the amplitude of the periodic jitter to a large value, for example 100 UI.

   :OUTJ:JITT:PER:AMPL 100; *OPC?

   It will take approximately 42 seconds to set the PJ amplitude from 0 UI to 100 UI at a PJ frequency = 1 Hz and about 18 seconds at
   PJ freq = 19 Hz.

10. Selecting a large RAM pattern

    Selecting a pattern to load onto the N4951A/N4951B or N4952A-E17/N4952A-E32 remote heads may take up to 11 minutes for an 8 Mb RAM pattern. Note, however, that loading PRBS patterns is fast.

11. Synchronization followed by an operation complete query (*OPC?)

    Synchronization is the process of aligning the detector internal reference bit pattern with the input bit stream. The bus interface timeout needs to be modified to ensure that synchronization can complete without triggering a communication timeout. If a communication timeout occurs before an operation complete

query is read, the instrument GPIB remote interface will lock requiring a power cycle to recover.

12. Executing an auto alignment when using a LAN gateway

    When using a LAN gateway, ensure that the gateway timeout is set greater than the auto alignment execution time (approximately 6 seconds). If a communication timeout has occurred, repeated execution of an auto alignment will cause the instrument USB or GPIB remote interface to lock and requires a power cycle to recover.

7 Returning the N4960A to Keysight

If the N4960A serial BERT fails system verification and you cannot correct the problem, return it to Keysight Technologies for repair following the steps shown below.

1. Record all symptoms.
2. Contact Keysight Technologies at http://www.Keysight.com/find/assist.
3. Use the original packing material or comparable packing material to ship the instrument to Keysight Technologies.

8 Appendix A Preset State

The following settings are the default values after performing an instrument preset:

Table 39. N4960A serial BERT preset state

Setting	Preset State
10 MHz Reference	Auto
Clock Source	Internal
Delay Clock Amplitude	0.700 V
Delay Clock Coupling	AC
Delay Clock Delay	0.0 UI
Delay Clock Offset	0 V
Delay Clock Output Enable	Off
Delay Clock Source	System
Delay Clock Termination	0 V
Delay Frequency	See Frq (displays Frequency when Delay Clock Source set to System)
Divided Clock Amplitude	0.700 V
Divided Clock Coupling	AC
Divided Clock Divide By	4
Divided Clock Offset	0 V
Divided Clock Output Enable	Off
Divided Clock Termination	0 V
External Jitter	Off
Frequency	5 GHz
Jittered Clock Amplitude	0.700 V
Jittered Clock Coupling	AC
Jittered Clock Offset	0 V
Jittered Clock Output Enable	Off
Jittered Clock Termination	0 V
LB Gain	1.0 UI/V
PJ Amplitude	0.0 UI
PJ Enable	Off

Setting	Preset State
PJ Frequency	100 kHz
RJ Amplitude	0 mUI-rms
RJ Enable	Off
SJ1 Amplitude	0.0 UI
SJ1 Enable	Off
SJ1 Frequency	10 MHz
SJ2 Amplitude	0.0 UI
SJ2 Enable	Off
SJ2 Frequency	10 MHz
SSC Deviation	5000 ppm
SSC Enable	Off
SSC Frequency	33 kHz
SSC Type	Down

Table 40. Pattern generator preset state

Setting	Preset State
Amplitude	0.5 V
Crossover	50 %
Data Rate	10 Gb/s
Delay[2]	0.0 UI
Error Injection Rate	E-3
Error Rate Injection Enable	Off
External Jitter[1]	Off
LB Gain[1]	2.0 UI/V
Logic	CUSTom
Name	PRBS2^7-1
Offset	0.0 V
Output Enable	Off
Pattern	PRBS2^7-1
Pattern Invert	Off
Pattern Type	PRBS
PJ Amplitude[1]	0.0 UI
PJ Enable[1]	Off
PJ Frequency[1]	100 kHz
Post Cursor 1[3]	+00.00 dB

Setting	Preset State
Post Cursor 2[3]	+00.00 dB
Post Cursor 3[3]	+00.00 dB
Pre Cursor[3]	+00.00 dB
RJ Amplitude[1]	0 mUI-rms
RJ Enable[1]	Off
SJ1 Amplitude[1]	0.0 UI
SJ1 Enable[1]	Off
SJ1 Frequency[1]	10 MHz
SJ2 Amplitude[1]	0.0 UI
SJ2 Enable[1]	Off
SJ2 Frequency[1]	10 MHz
Termination	0.0 V

[1] Applies to pattern generator connected to Jitter connector (channel 0) on front panel of N4960A only.

[2] Applies to pattern generator connected to Delay connector (channel 1) on front panel of N4960A only.

[3] Applies to N4951B-D17/-D32 pattern generators only.

Table 41. Error detector preset state

Setting	Preset State
Auto Pattern	Off
BER Thrshld	1E-2
Delay	0.0 UI
Delay Step	20 mUI
Name	PRBS2^7-1
Pattern	PRBS2^7-1
Pattern Invert	Off
Pattern Type	PRBS
Sample Voltage	0.0 V
Sample Voltage Step	20 mV
Set Delay	On
Set Sample Voltage	On
Stop	Manual
Stop Criteria - Bits	E8
Stop Criteria - Duration	10 seconds
Stop Criteria - Errors	1
Sync Mode	Auto
Termination Voltage	0.0 V

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